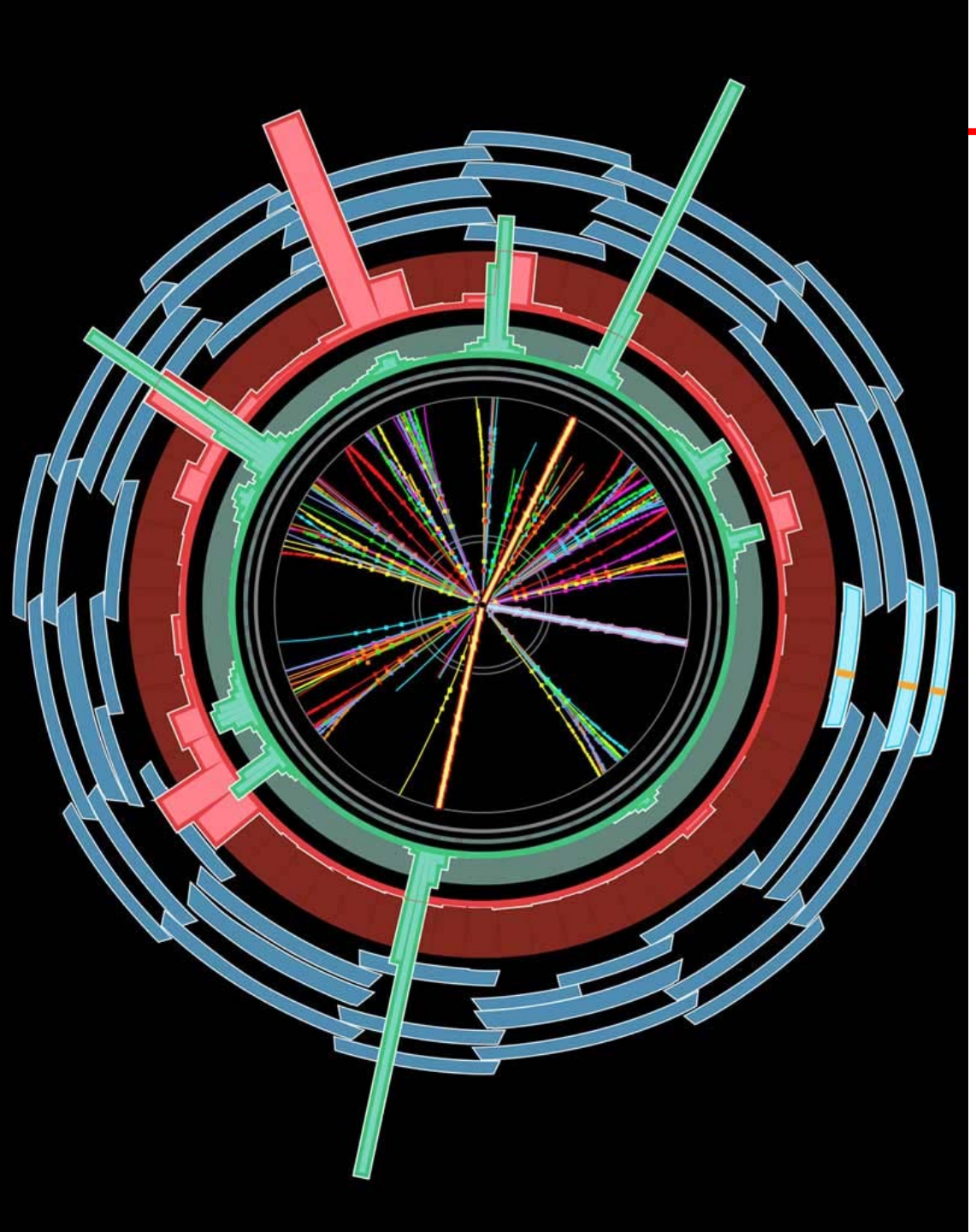


Electronics in particle physics

C. de LA TAILLE

LAL Orsay

Taille@lal.in2p3.fr

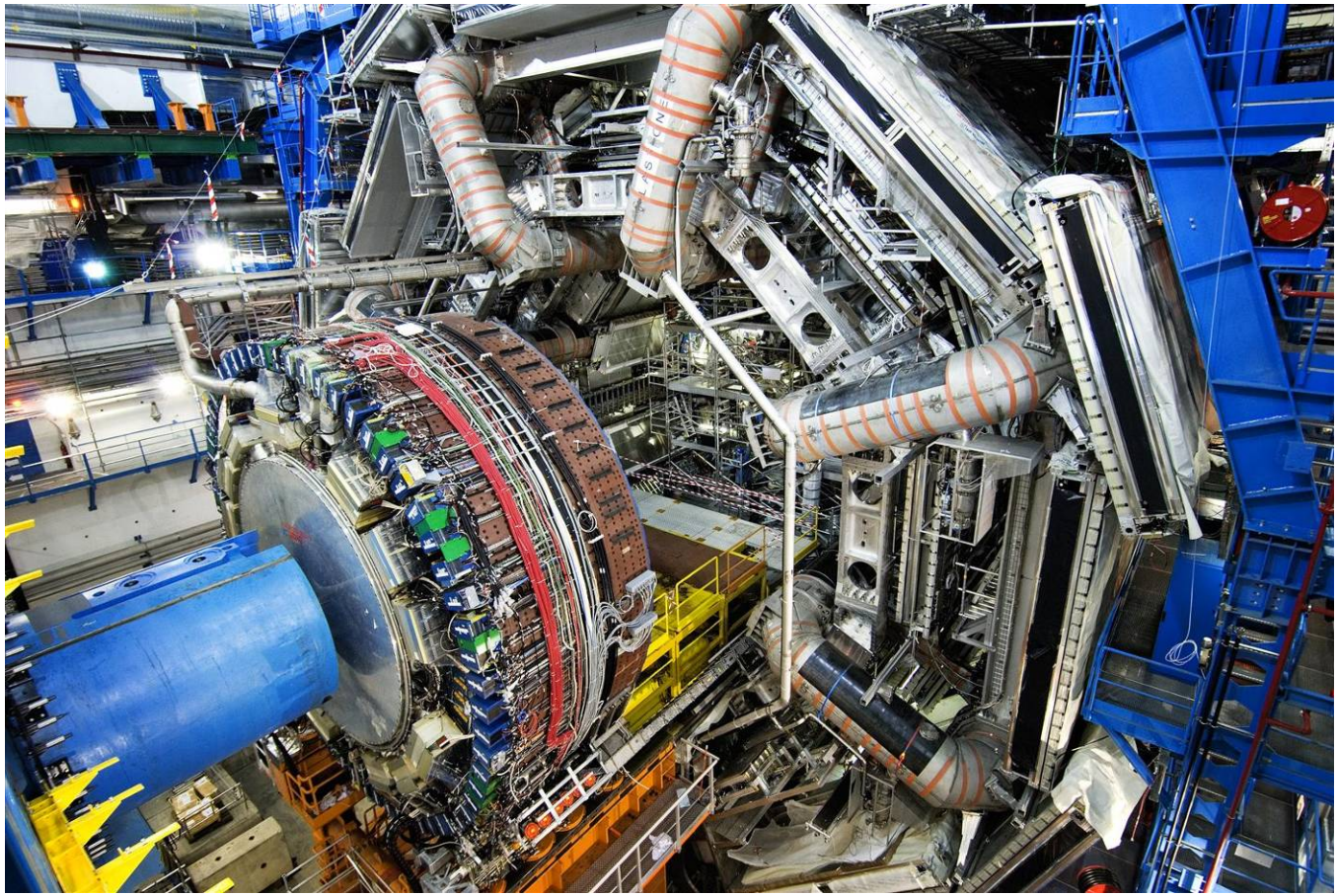
CNRS CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

IN2P3 INSTITUT NATIONAL DE PHYSIQUE NUCLÉAIRE ET DE PHYSIQUE DES PARTICULES

LAL LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Electronics in experiments

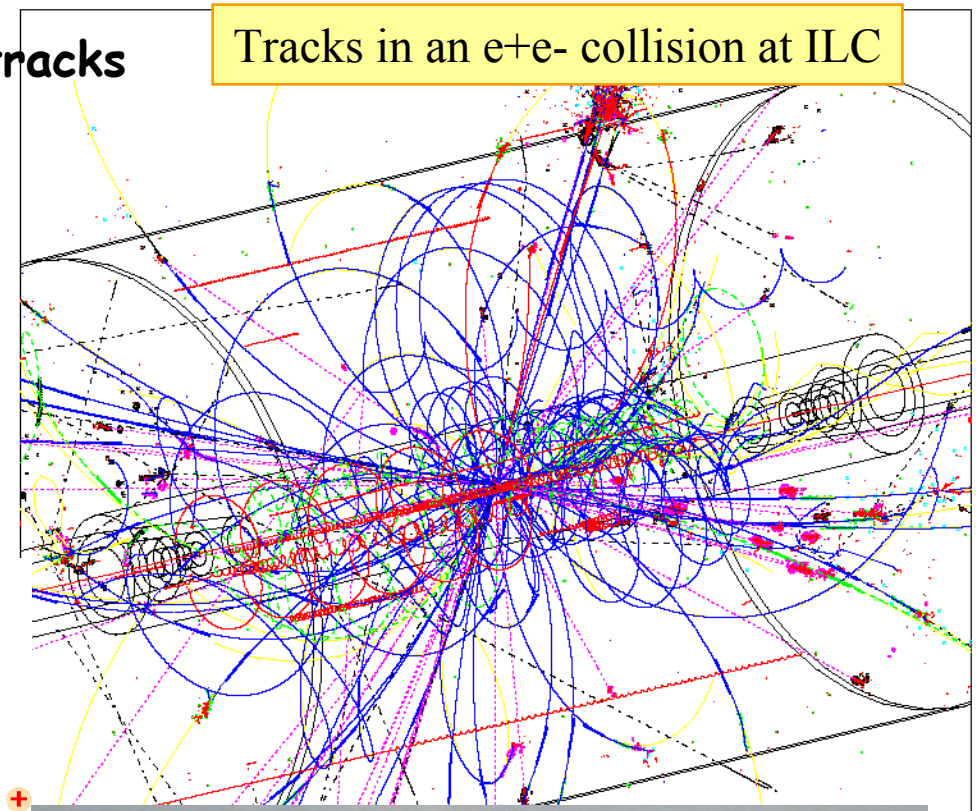
- **A lot of electronics in the experiments…**
  - Readout electronics : amplification, filtering… : Analog electronics (A,V,C)
  - Processing & Trigger electronics : Digital electronics (bits)
  - The performance of electronics often impacts on the detectors

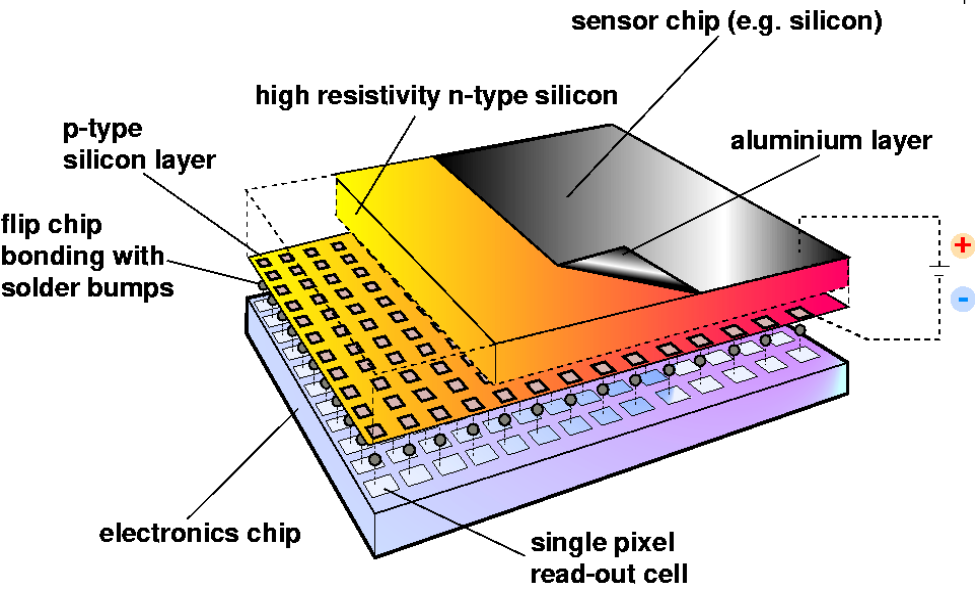


Electronics allowing better detectors : trackers

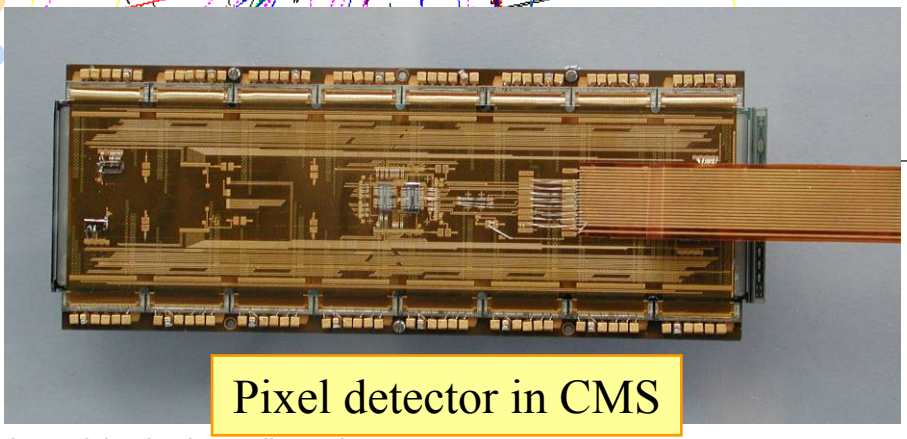
- **Measurement of (charged) particle tracks**
  - millions of pixels (~100 μm)
  - (quasi) binary readout at 40 MHz
  - High radiation levels
  - Made possible by ASICs

Tracks in an e+e- collision at ILC





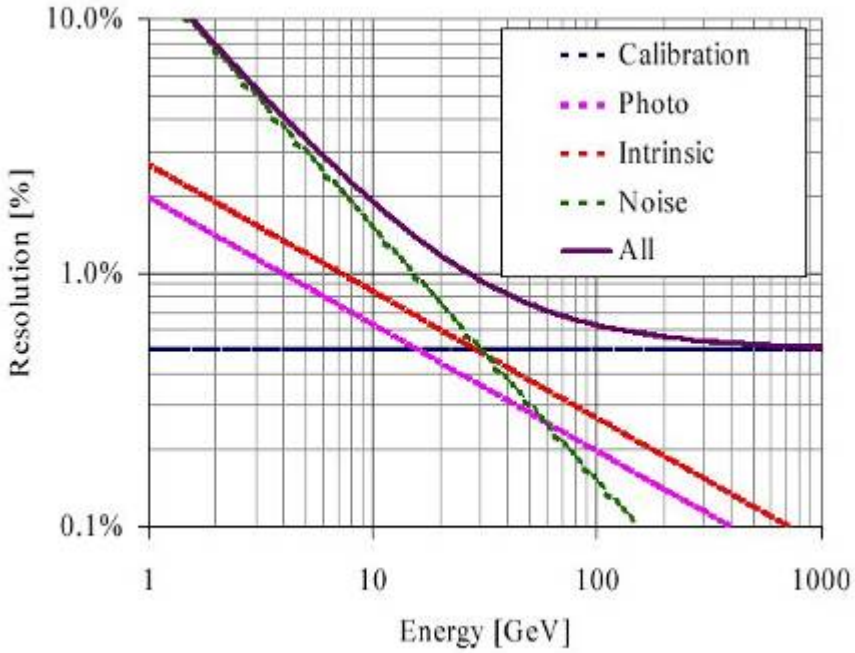
Pixel detector and readout electronics



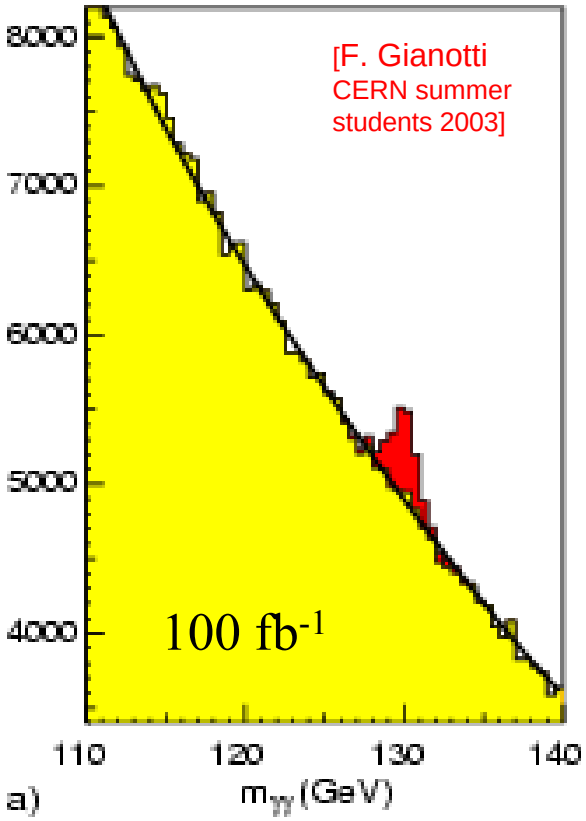
Pixel detector in CMS

Importance of electronics : calorimeters

- **Calorimetry = energy measurement** (≈ mass)
- **Dynamic range : maximum signal/minimum signal (or noise)**
  - Typically : 10^3 – 10^5
  - Often specified in dB (=20log Vmax/Vmin) = 60 – 100 dB
  - Also in bits : 2^n = Vmax/vmin = 10 – 18 bits
- **Precision ~1%**
  - Energy resolution : **σ(E)**
  - Importance of low noise, uniformity, linearity…

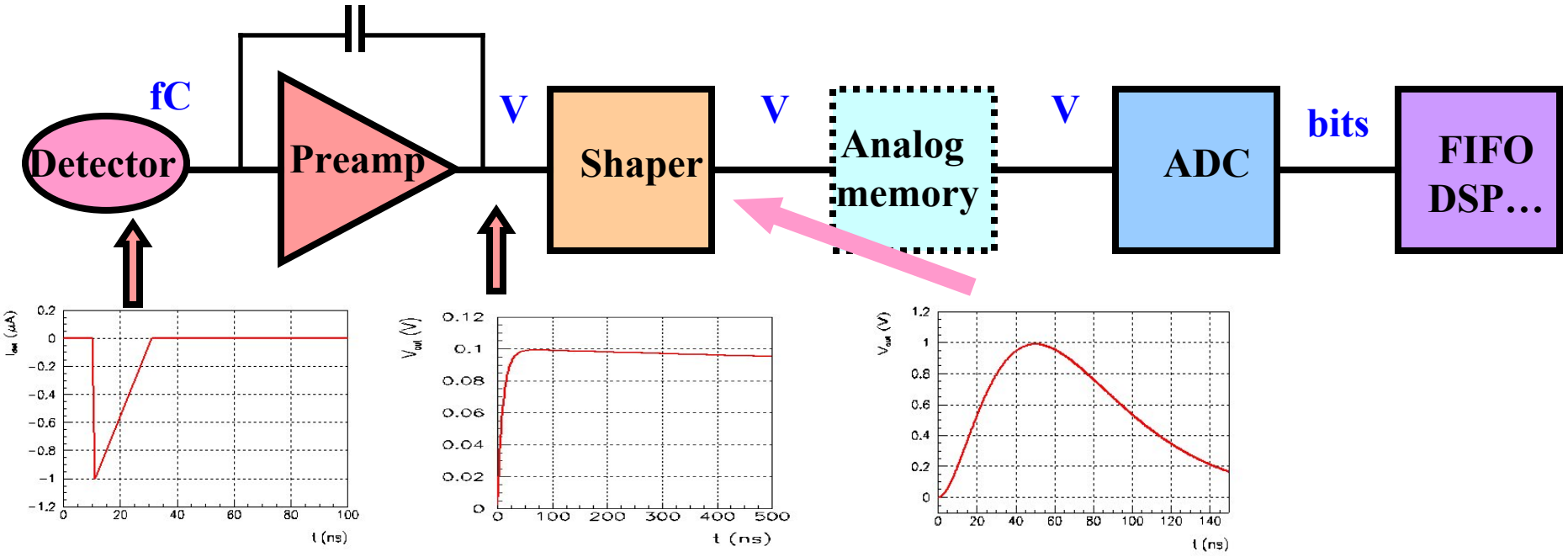


H-> γ γ in CMS calorimeter



Overview of readout electronics

- Most front-ends follow a similar architecture



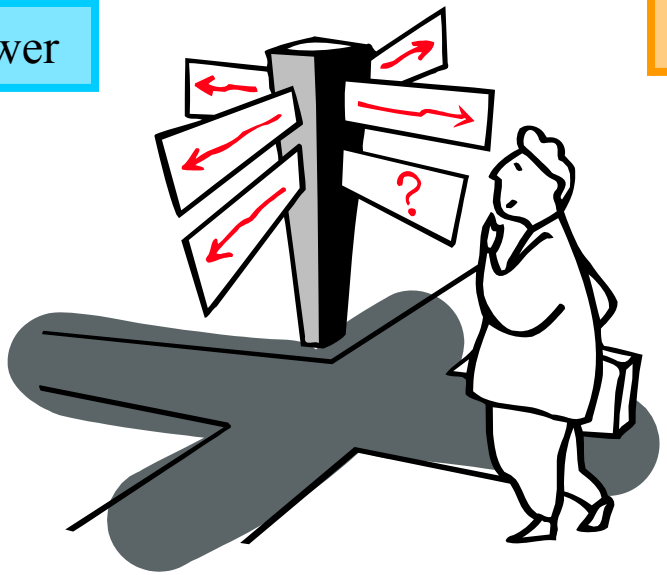
- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels

Readout electronics : requirements

Low noise

Low power

High speed



High reliability

Large dynamic range

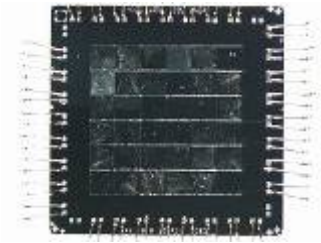
Radiation hardness

Low material

Low cost !
(and even less)

Detector(s)

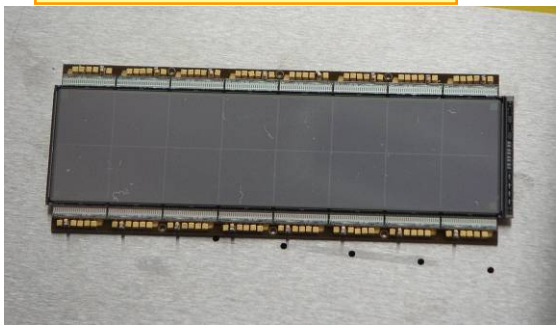
- A large variety
- A similar modelization

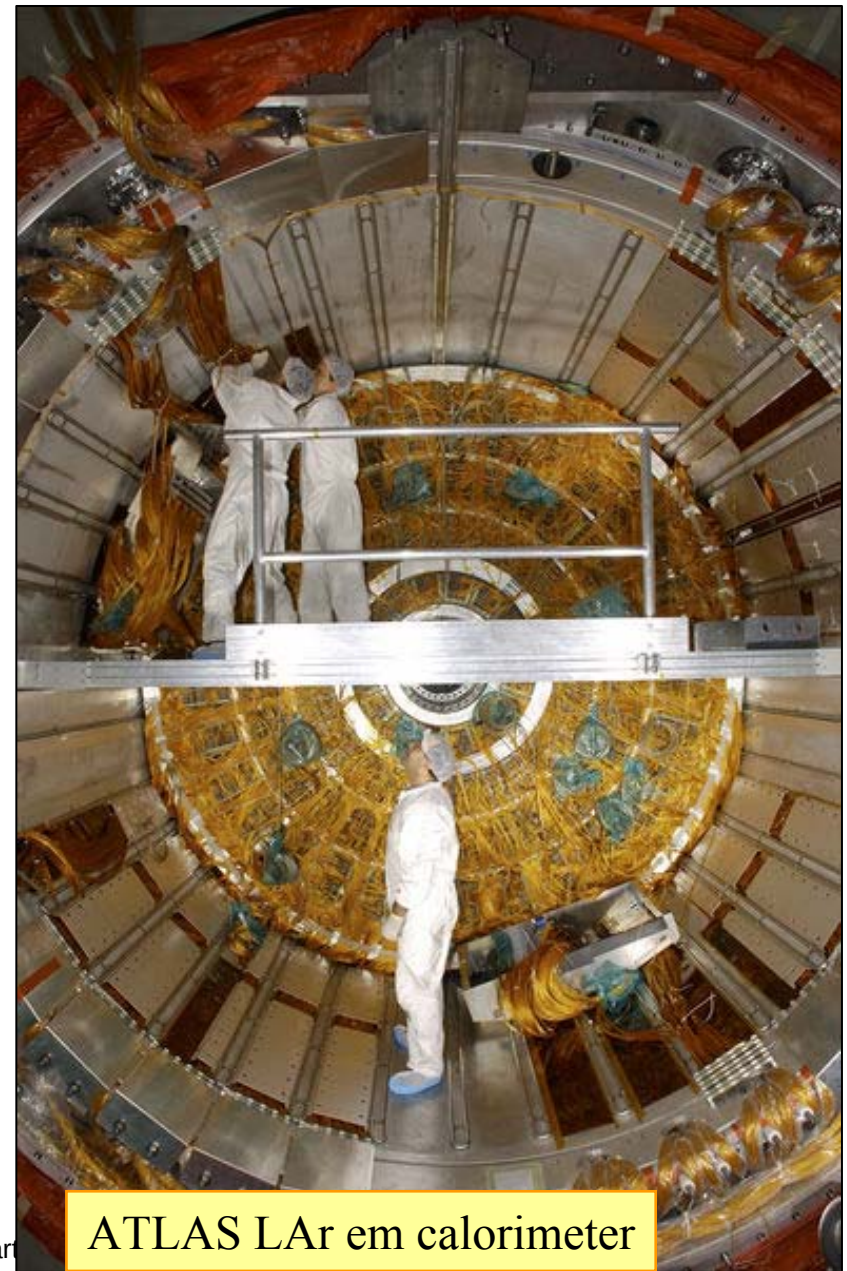


6x6 pixels,4x4 mm^2
HgTe absorbers, 65 mK
12 eV @ 6 keV

PMT for Antares

CMS Pixel module

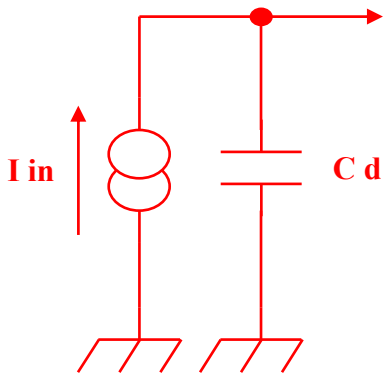




ATLAS LAr em calorimeter

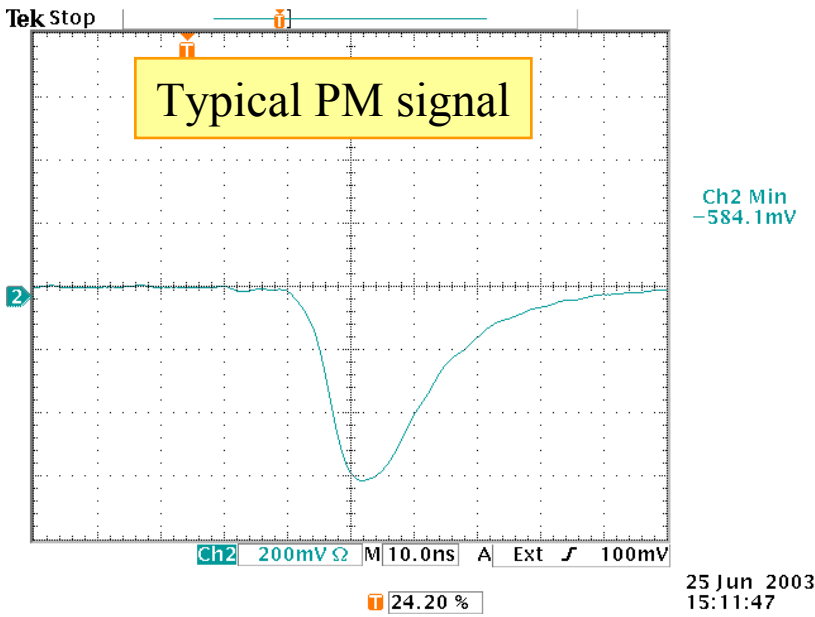
Detector modelization

- **Detector = capacitance Cd**
  - Pixels : 0.1-10 pF
  - PMs : 3-30pF
  - Ionization chambers 10-1000 pF
  - Capa or transmission line?



Detector modelisation

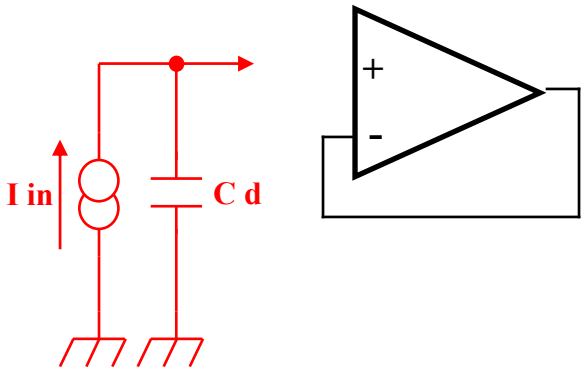
- **Signal : current source**
  - Pixels : ~100e-/µm
  - PMs : 1 photoelectron -> 10^5-10^7 e-
  - Modelized as an impulse (Dirac) : $i(t)=Q_0\delta(t)$



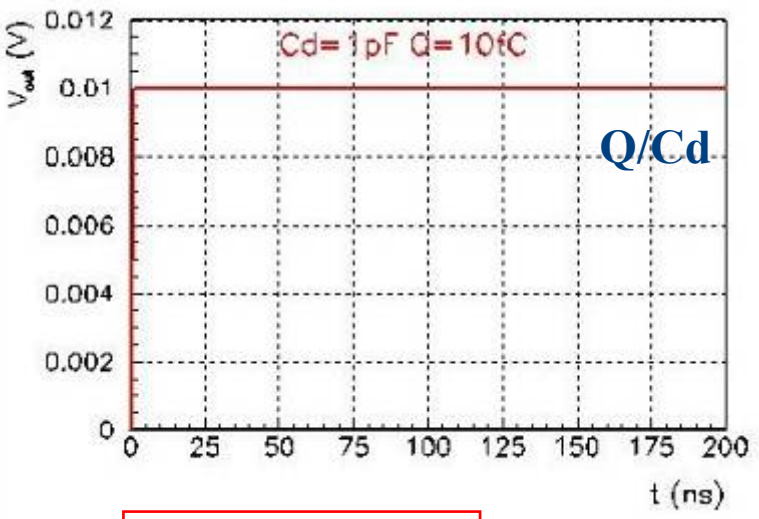
- **Missing :**
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration…

Reading the signal

- **Signal**
  - Signal = current source
  - Detector = capacitance C_d
  - Quantity to measure
    - Charge => integrator needed
    - Time => discriminator + TDC

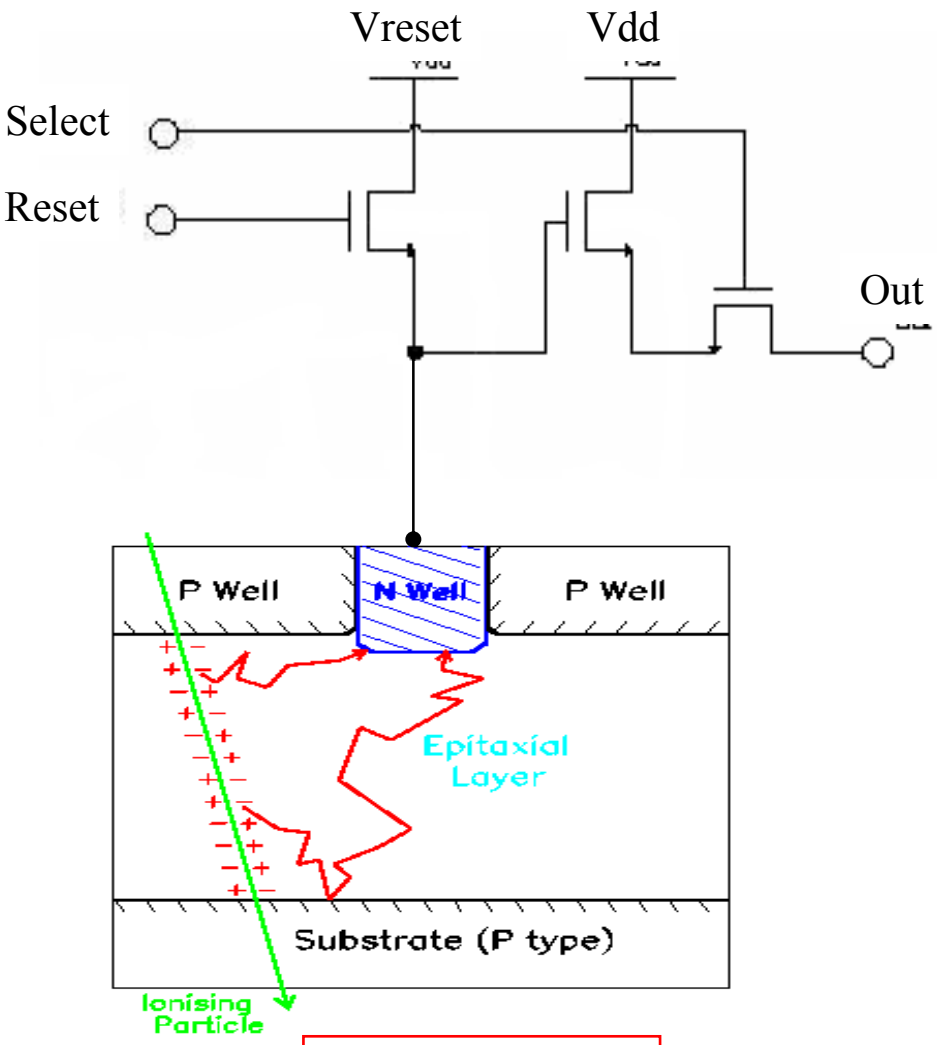


- **Integrating on Cd**
  - Simple : $V = Q/C_d$
  - « Gain » : $1/C_d$: 1 pF -> 1 mV/fC
  - Need a follower to buffer the voltage…
  - Input follower capacitance : Ca // Cd
  - Gain loss, possible non-linearities
  - crosstalk
  - Need to empty Cd…

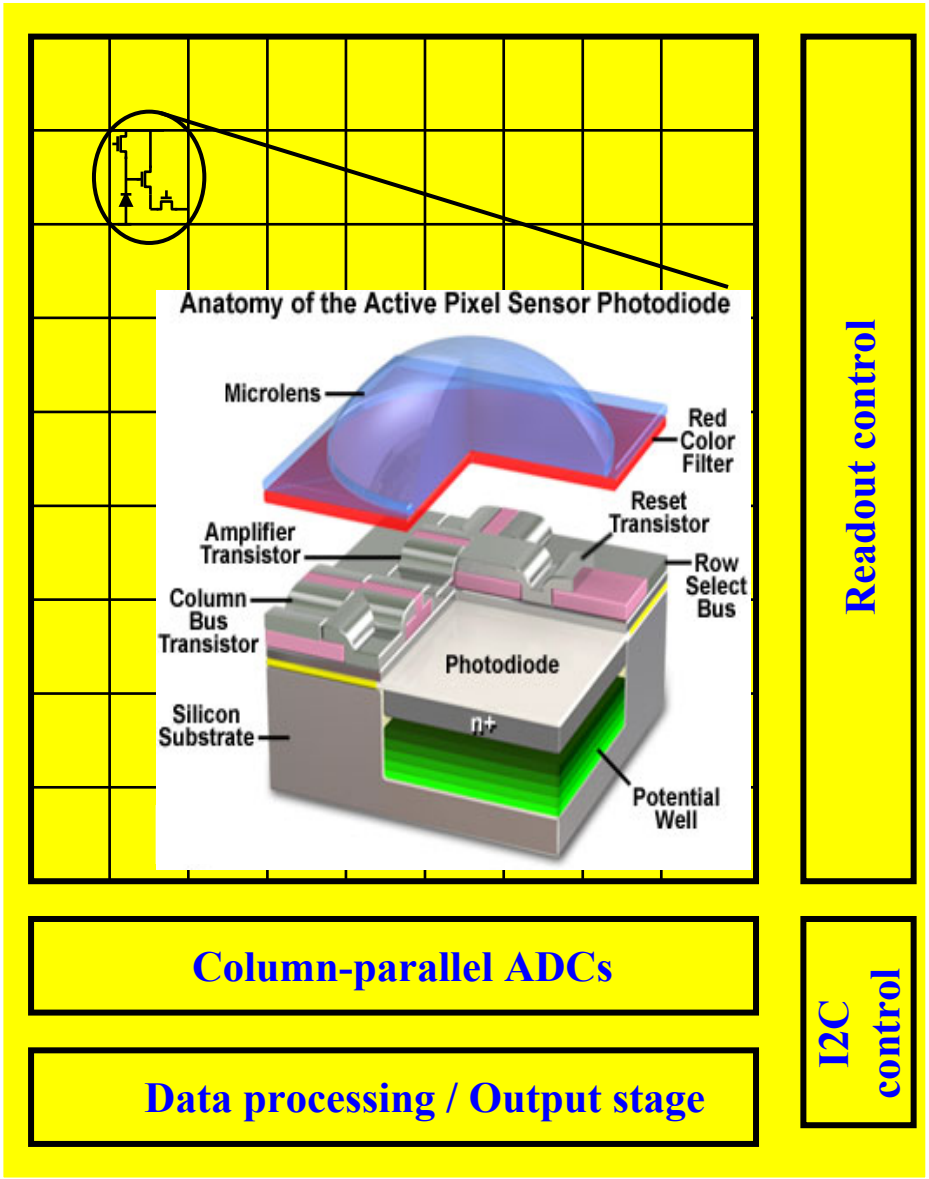


Impulse response

Monolithic active pixels



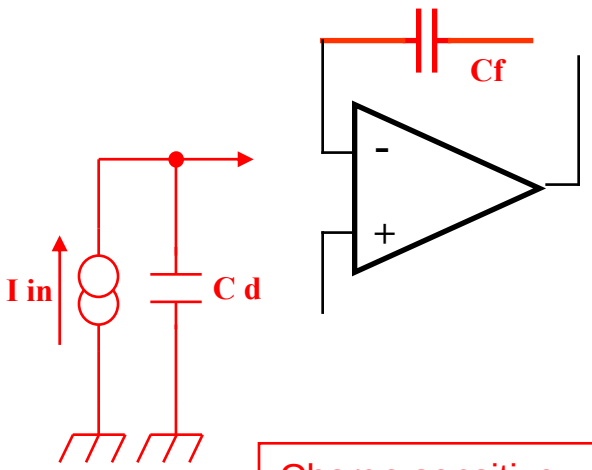
MAPS readout



Ideal charge preamplifier

- **ideal opamp in transimpedance**
  - Shunt-shunt feedback
  - transimpedance : v_{out}/i_{in}
  - Vin-=0 =>$V_{out}(\omega)/i_{in}(\omega) = - Z_f = - 1/j\omega C_f$
  - Integrator : $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

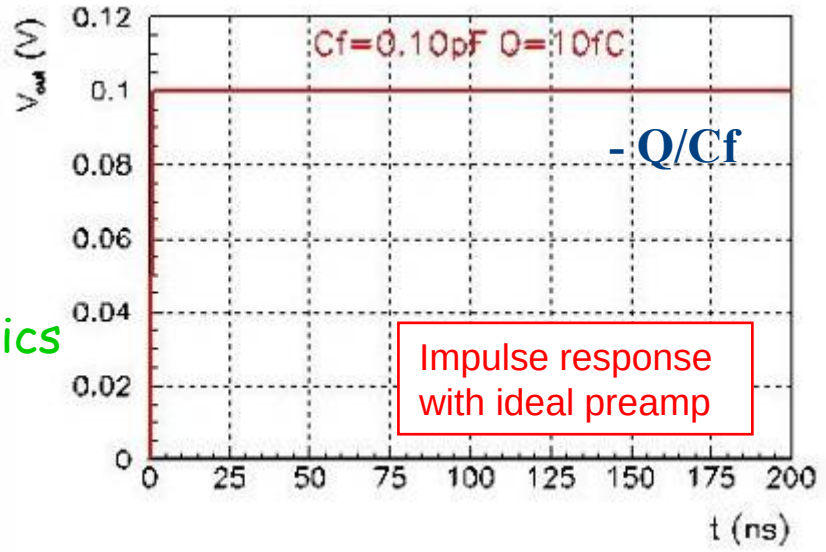
$$v_{out}(t) = - Q/C_f$$



Charge sensitive preamp

  - « Gain » : $1/C_f$: 0.1 pF -> 10 mV/fC
  - C_f determined by maximum signal

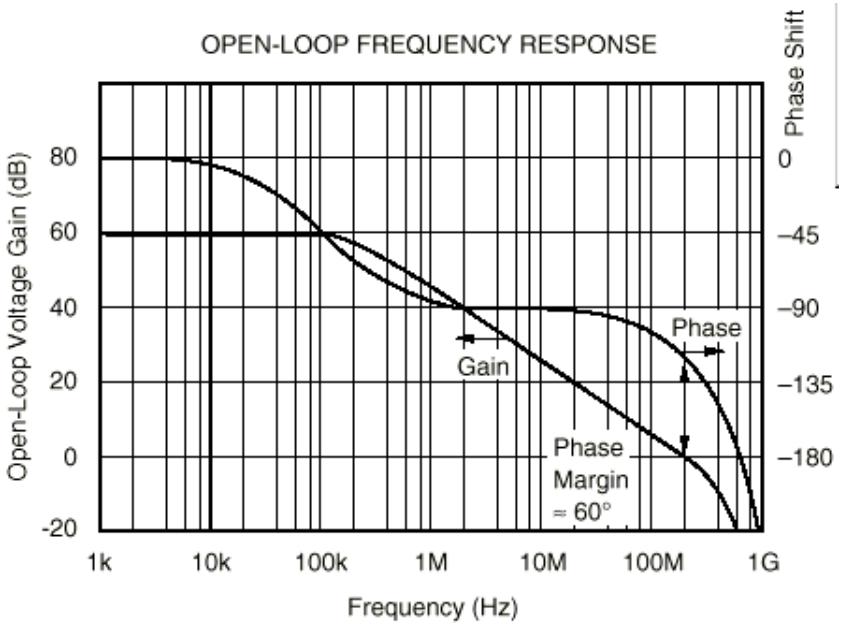
- **Integration on Cf**
  - Simple : $V = - Q/C_f$
  - Unsensitive to preamp capacitance C_{PA}
  - Turns a short signal into a long one
  - The front-end of 90% of particle physics detectors…
  - But always built with custom circuits…

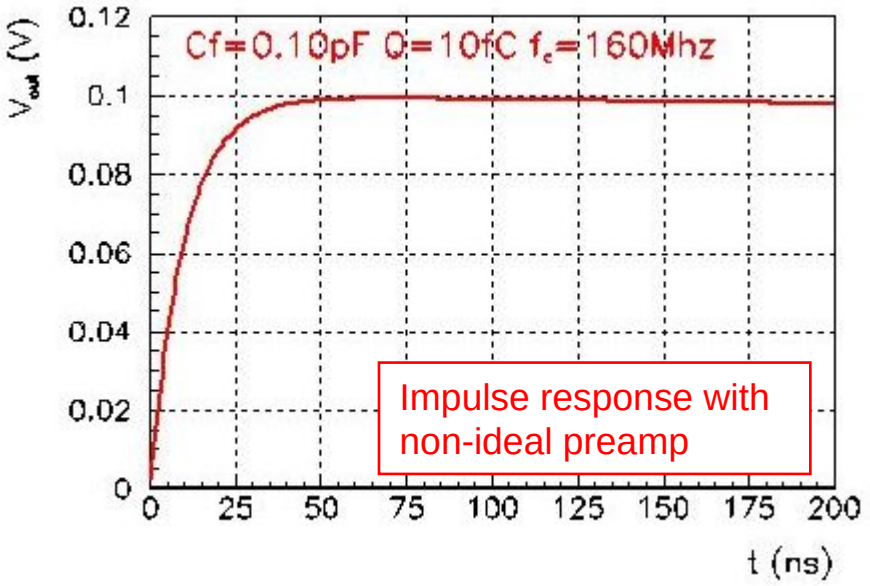


Impulse response with ideal preamp

Non-ideal charge preamplifier

- **Finite opamp gain**
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + C_d / G_0 C_f)$
  - Small signal loss in $C_d / G_0 C_f \ll 1$ (ballistic deficit)
- **Finite opamp bandwidth**
  - First order open-loop gain
  - $G(\omega) = G_0/(1 + j\, \omega/\omega_0)$
    - G_0 : low frequency gain
    - $G_0\omega_0$: gain bandwidth product
- **Preamp risetime**
  - Due to gain variation with ω
  - Time constant : τ *(tau)* = $C_d / G_0\omega_0 C_f$
  - Rise-time : $t_{10\text{-}90\%} = 2.2\ \tau$
  - Rise-time optimised with $w_{C\ or}\ C_f$





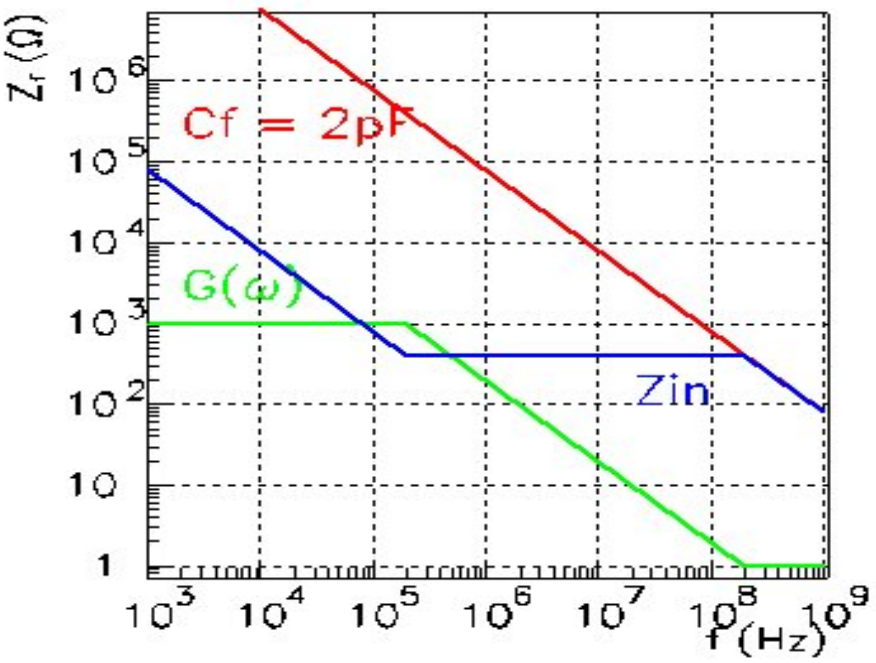
Charge preamp seen from the input

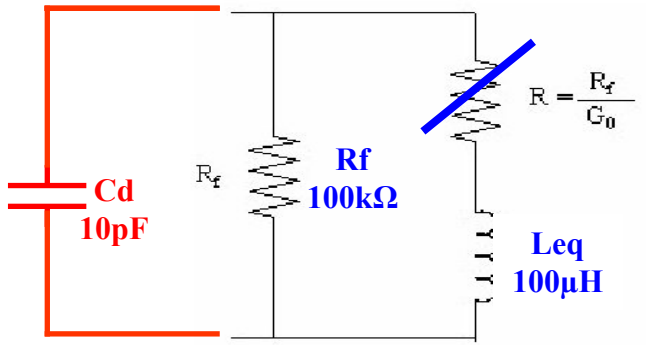
- **Input impedance with ideal opamp**
  - Zin = Zf / G+1
  - Zin->0 for ideal opmap
  - « Virtual ground » : Vin = 0
  - Minimizes sensitivity to detector impedance
  - Minimizes crostalk

- **Input impedance with real opamp**
  - Zin = $1/j\omega\, G_0 C_f + 1/ G_0\omega_0 C_f$
  - Resistive term : $Rin = 1/ G_0\omega_0 C_f$
    - Exemple : $w_c = 10^9$ rad/s C_f= 0.1 pF => Rin = 10 k
  - Determines the input time constant : $t = R_{eq}C_d$
  - Good stability= (…!)

- **Equivalent circuit :**

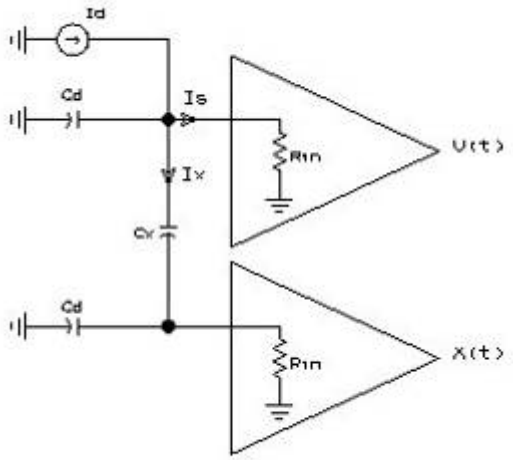
Input impedance or charge preamp



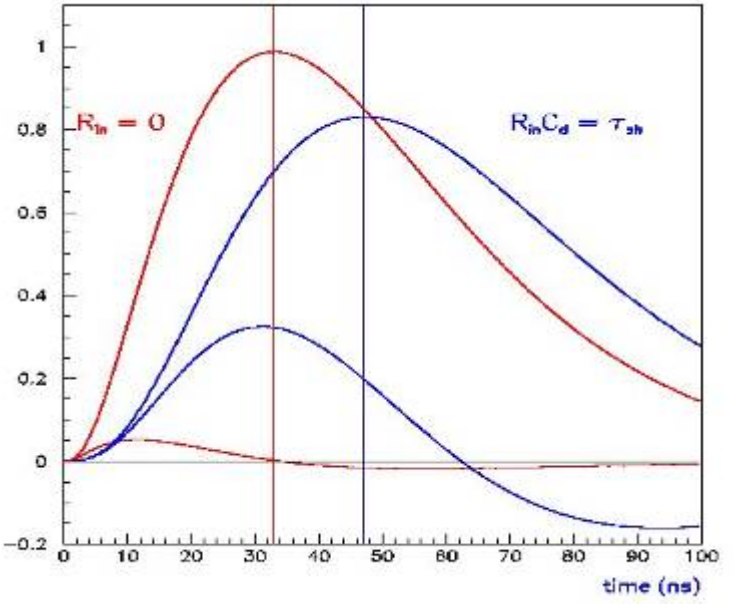


Crosstalk

- **Capacitive coupling between neighbours**
  - Crosstalk signal is differentiated and with same polarity
  - Small contribution at signal peak
  - Proportionnal to Cx/Cd and preamp input impedance
  - Slowed derivative if RinCd ~ tp => non-zero at peak

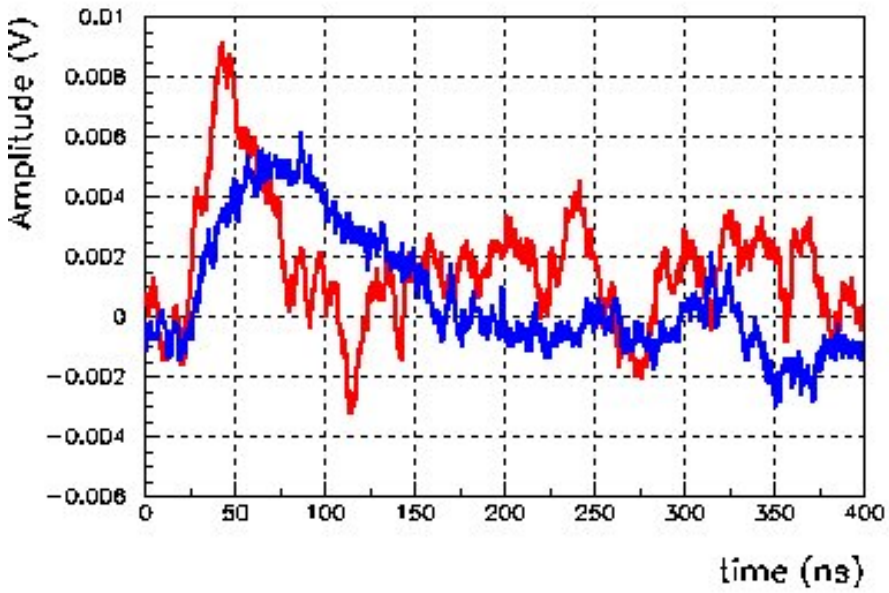


- **Inductive coupling**
  - Inductive common ground return
  - "Ground apertures" = inductance
  - Connectors : mutual inductance



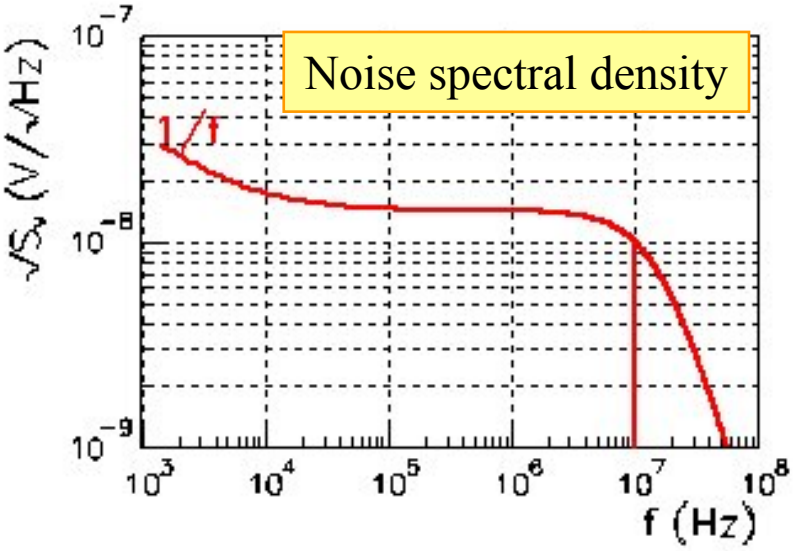
Electronics noise

- **Definition of Noise**
  - Random fluctuation superposed to interesting signal
  - Statistical treatment
- **Three types of noise**
  - Fundamental noise (Thermal noise, shot noise)
  - Excess noise (1/f …)
  - Parasitics -> EMC/EMI (pickup noise, ground loops…)

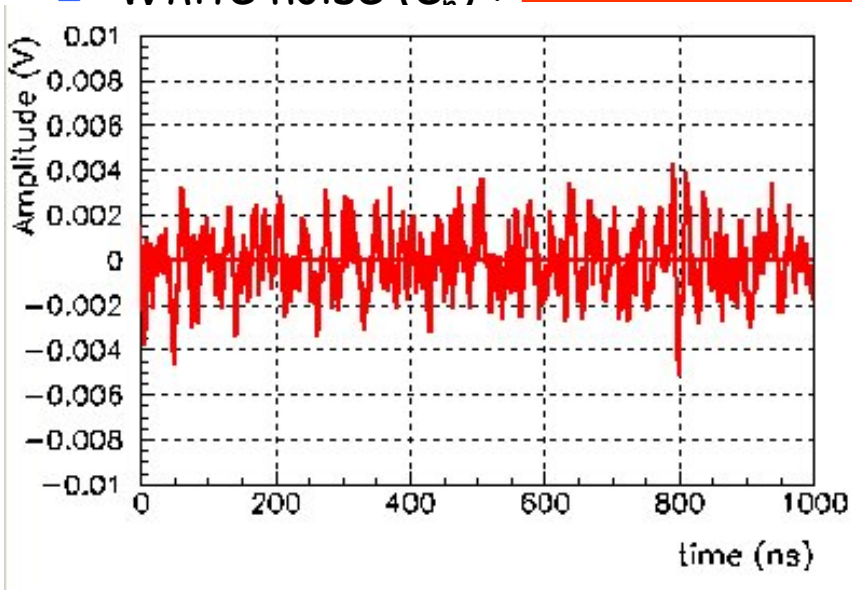


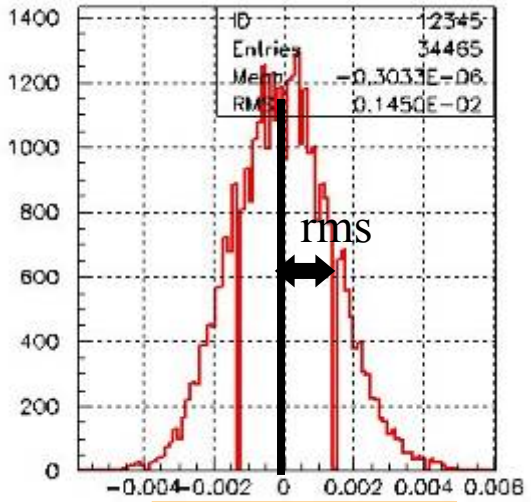
Electronics noise

- **Modelization**
  - Noise generators : e_n, i_n,
  - Noise spectral density of e_n & i_n : $S_v(f)$ & $S_i(f)$
  - Sv(f) = $|\ \mathcal{F}(e_n)\ |^2$ (V^2/Hz)



- ***Rms* noise Vn**
  - $V_n^2 = \int e_n^2(t)\,dt = \int Sv(f)\,df$
  - White noise (e_n) : $v_n = e_n \sqrt{\frac{1}{2}\pi f_{-3dB}}$

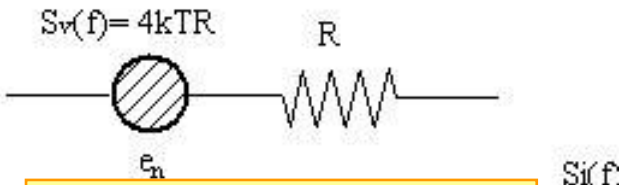




Rms noise vn

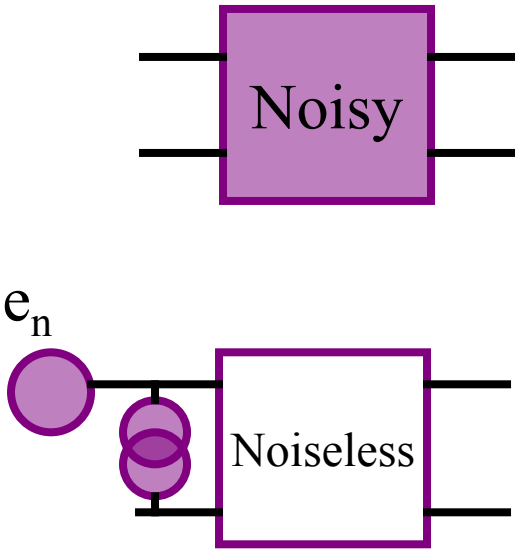
Calculating electronics noise

- **Fundamental noise**
  - Thermal noise (resistors) : Sv(f) = 4kTR
  - Shot noise (junctions) : Si(f) = 2qI



Thermal noise generator

- **Noise referred to the input**
  - All noise generators can be referred to the input as 2 noise generators :
  - A voltage one e_n in series : series noise
  - A current one i_n in parallel : parallel noise
  - Two generators : no more, no less… why ?
    - To take into account the Source impedance

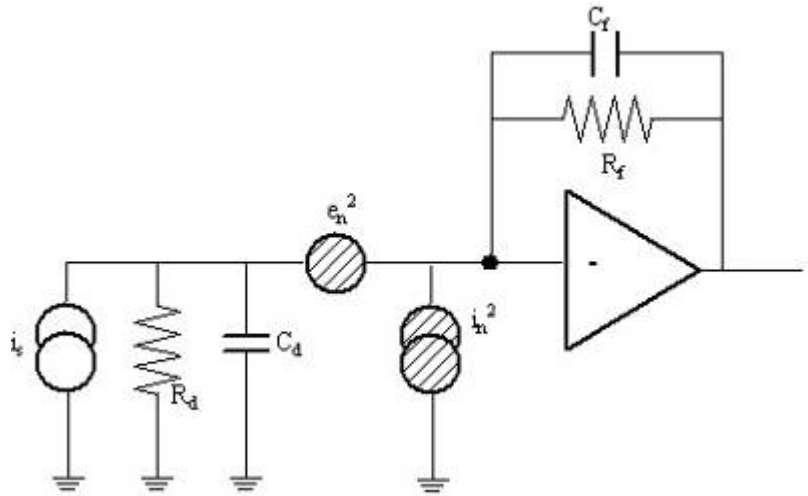


Noise generators referred to the input

- **Golden rule**
  - Always calculate the signal before the noise what counts is the signal to noise ratio
  - Don't forget noise generators are V^2/Hz => calculations in module square
  - Practical exercice next slide

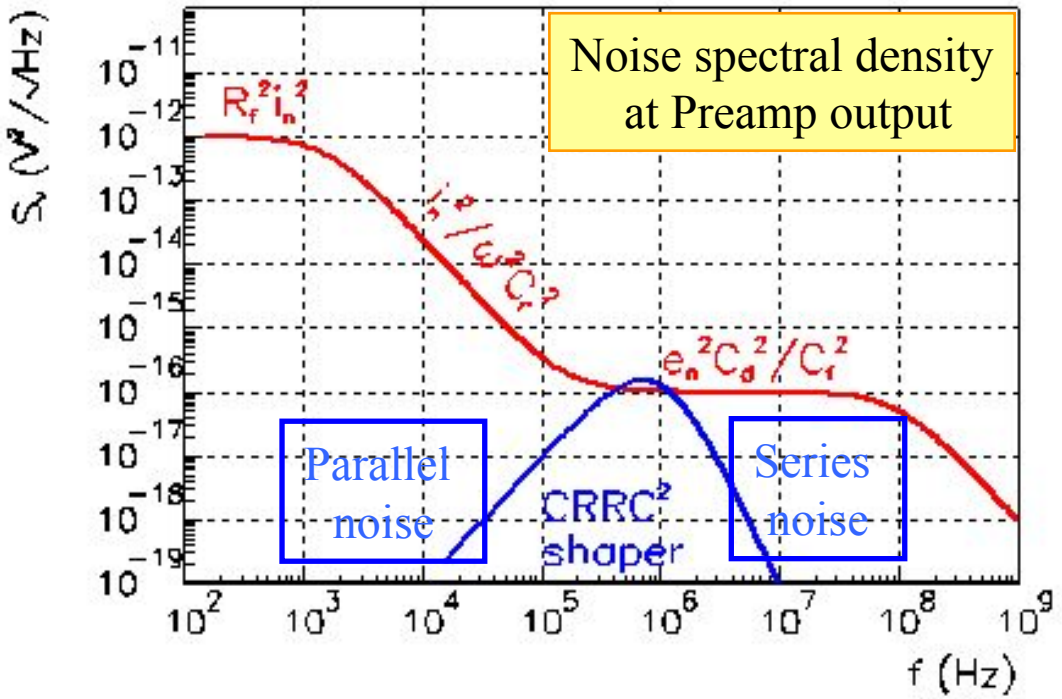
Noise in charge pre-amplifiers

- **2 noise generators at the input**
  - Parallel noise : (i_n^2) (leakage currents)
  - Series noise : (e_n^2) (preamp)



- **Output noise spectral density :**
  - $Sv(\omega) = (i_n^2 + e_n^2/|Z_d|^2) / \omega^2 C_f^2$
    $= i_n^2 /\omega^2 C_f^2 + e_n^2 C_d^2/C_f^2$
  - Parallel noise in $1/\omega^2$
  - Series noise is flat, with a « noise gain » of C_d/C_f

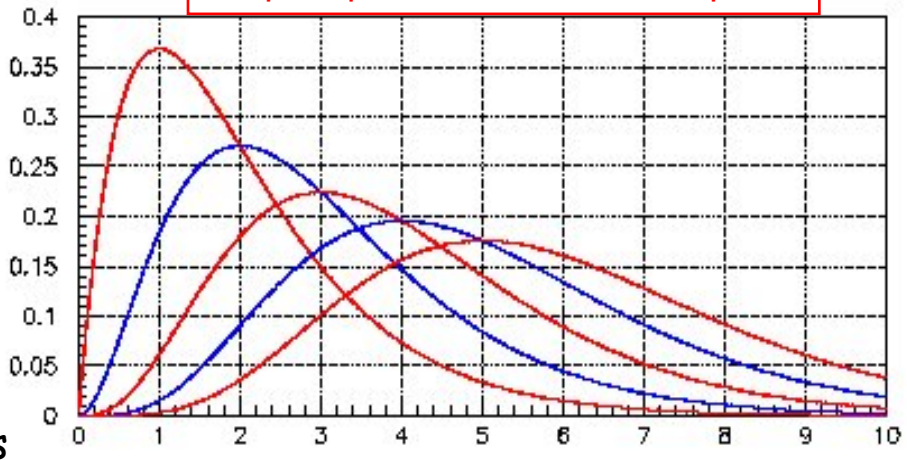
- ***rms* noise V_n**
  - $V_n^2 = \int Sv(\omega)\, d\omega/2\pi \rightarrow \infty$ (!)
  - Benefit of shaping…



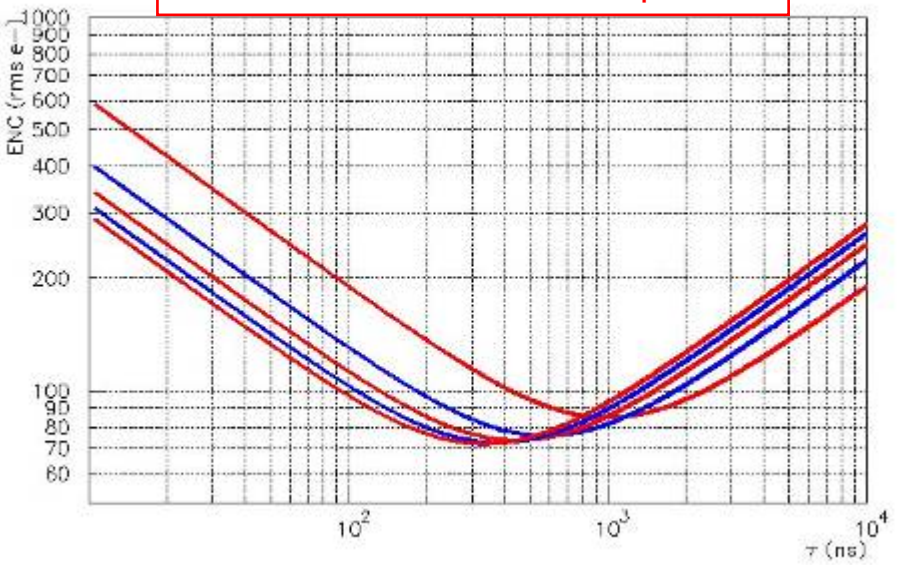
Equivalent Noise Charge (ENC) after CRRC^n

- **Noise reduction by optimising useful bandwidth**
  - Low-pass filters (**RC^n**) to cut-off high frequency noise
  - High-pass filter (**CR**) to cut-off parallel noise
  - -> pass-band filter CRRC^n
- **Equivalent Noise Charge : ENC**
  - Noise referred to the input in electrons
  - ENC = Ia(n) $e_n C_t/\sqrt{\tau} \oplus$ Ib(n) $i_n * \sqrt{\tau}$
  - Series noise in $1/\sqrt{\tau}$
  - Paralle noise in $\sqrt{\tau}$
  - 1/f noise independant of τ
  - Optimum shaping time $\tau_{opt} = \tau_c/\sqrt{2n-1}$
- **Peaking time tp (5-100%)**
  - ENC(**tp**) independent of n
- **Complex shapers are obsolete :**
  - Power of digital filtering
  - Analog filter = CRRC ou CRRC^2

Step response of CR RCn shapers



ENC vs tau for CR RCn shapers



Equivalent Noise Charge (ENC) after CRRC^n

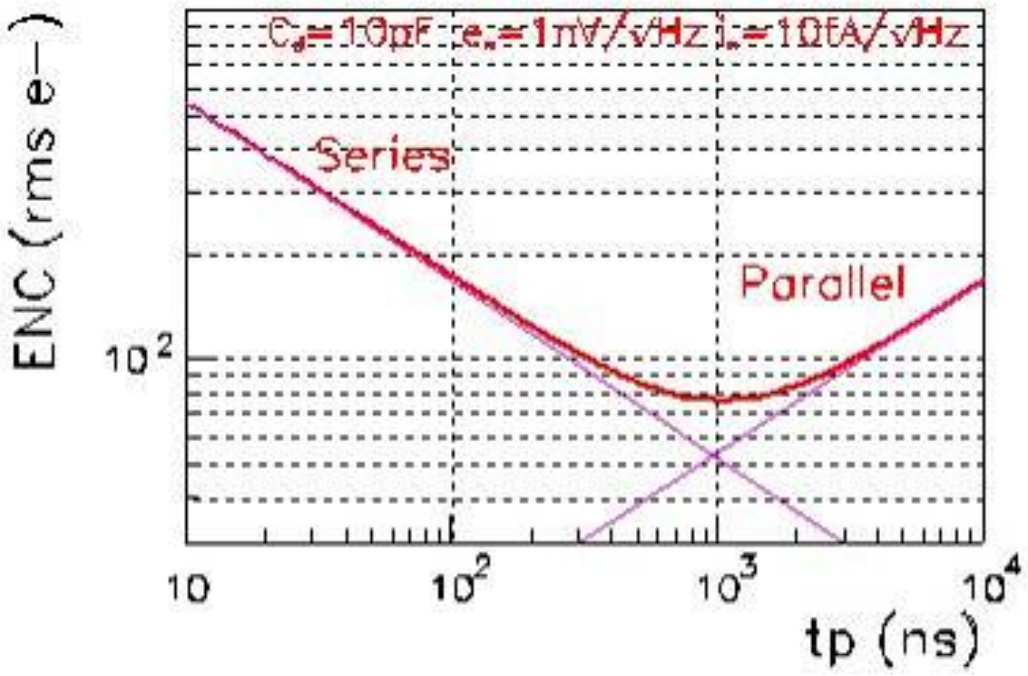
- **A useful formula** : ENC (e- rms) after a CRRC^2 shaper :

$$ENC = 174\ e_n C_{tot}/\sqrt{t_p}\ (\delta) \oplus 166\ i_n \sqrt{t_p}\ (\delta)$$

  - e_n in nV/ √Hz, i_n in pA/ √Hz are the preamp noise spectral densities
  - C_{tot} (in pF) is dominated by the detector (C_d) + input preamp capacitance (C_{PA})
  - t_p (in ns) is the shaper peaking time (5-100%)

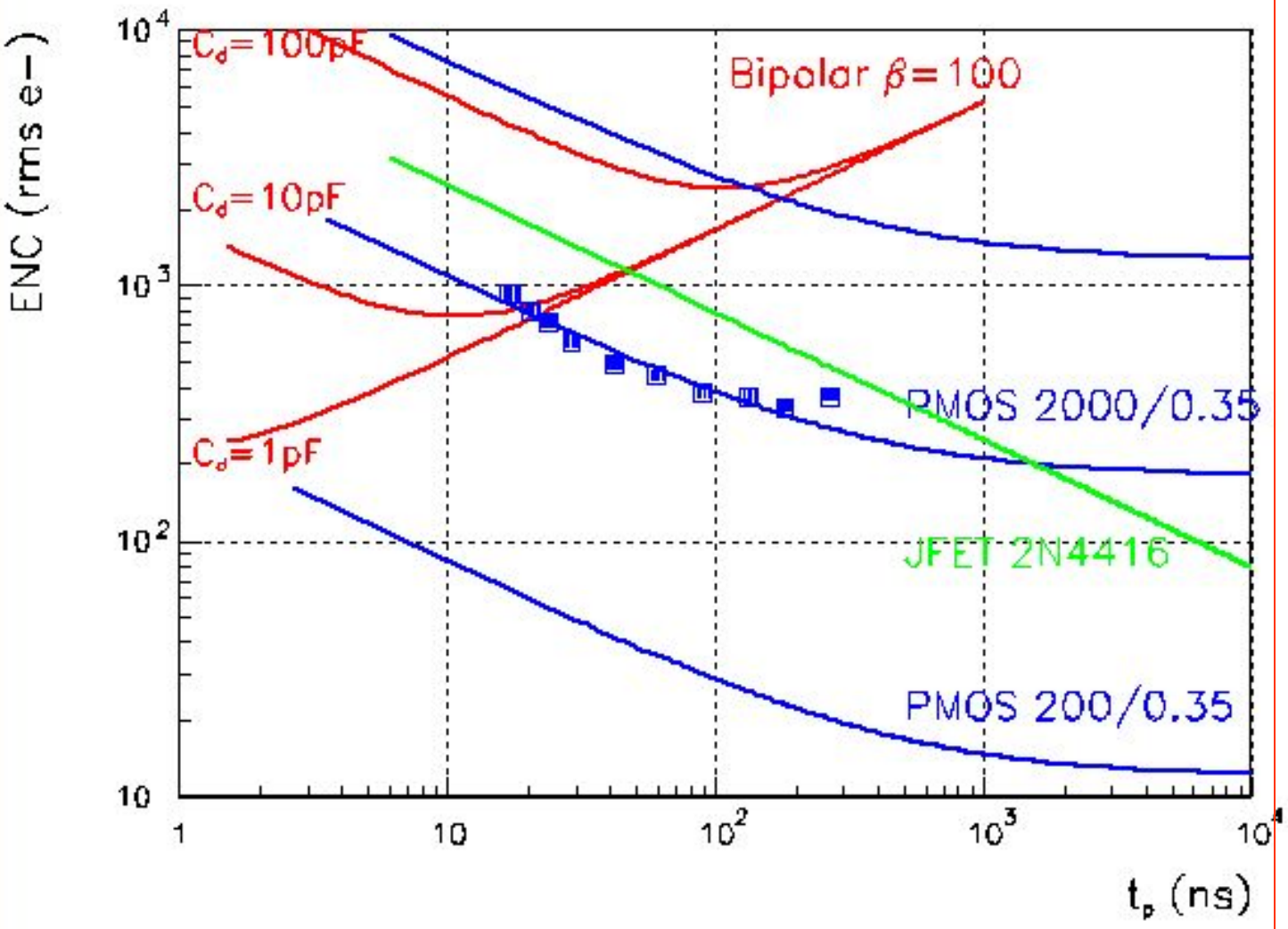
- **Noise minimization**
  - Minimize source capacitance
  - Operate at optimum shaping time
  - Preamp series noise (en) best with high trans-conductance (g_m) in input transistor

    => large current, optimal size



ENC for various technologies

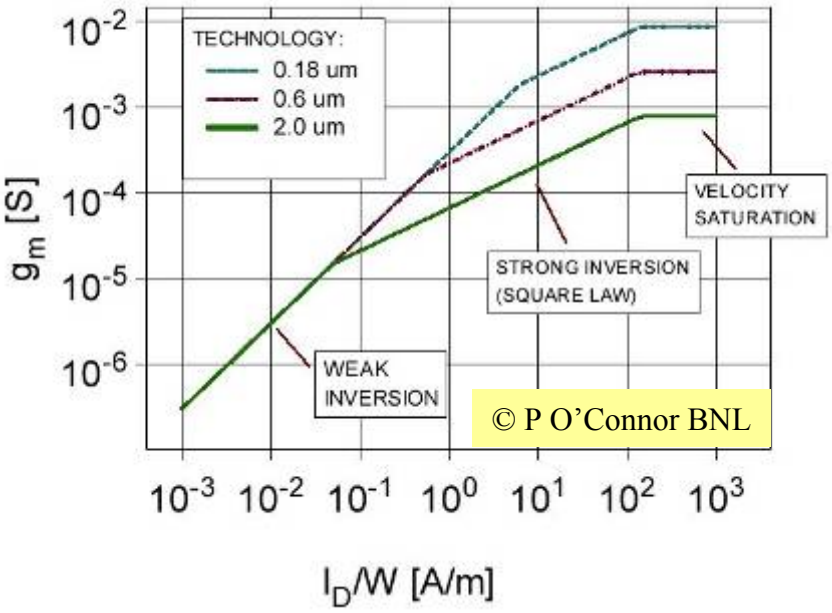
- **ENC for Cd=1, 10 and 100 pF at I_D = 500 uA**
  - MOS transistors best between 20 ns – 2 µs



- **Parameters**
- Bipolar :
  - g_m = 20 mA/V
  - $R_{BB'}$=25 Ω
  - e_n= 1 nV/√Hz
  - I_B=5uA
  - i_n = 1 pA/√Hz
  - C_{PA}=100fF
- **PMOS 2000/0.35**
  - g_m = 10 mA/V
  - e_n = 1.4 nV/√Hz
  - C_{PA} = 5 pF
  - 1/f :

MOS input transistor sizing

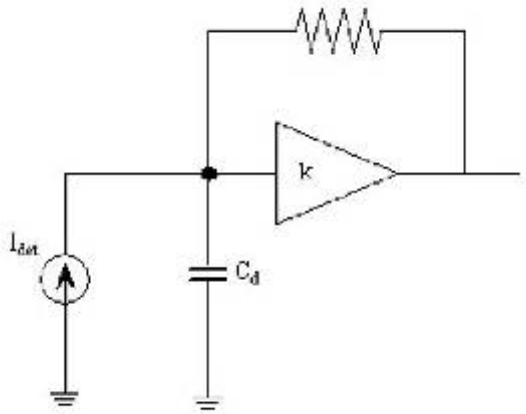
- **Capacitive matching : strong inversion**
  - g_m proportionnal to $W/L \sqrt{I_D}$
  - C_{GS} proportionnal to W*L
  - ENC propotionnal to $(Cdet+C_{GS})/\sqrt{gm}$
  - Optimum W/L : C_{GS} = 1/3 Cdet
  - Large transistors are easily in moderate or weak inversion at small current



- **Optimum size in weak inversion**
  - g_m proportionnal to I_D (indep of W,L)
  - ENC minimal for C_{GS} minimal, provided the transistor remains in weak inversion

Current preamplifiers :

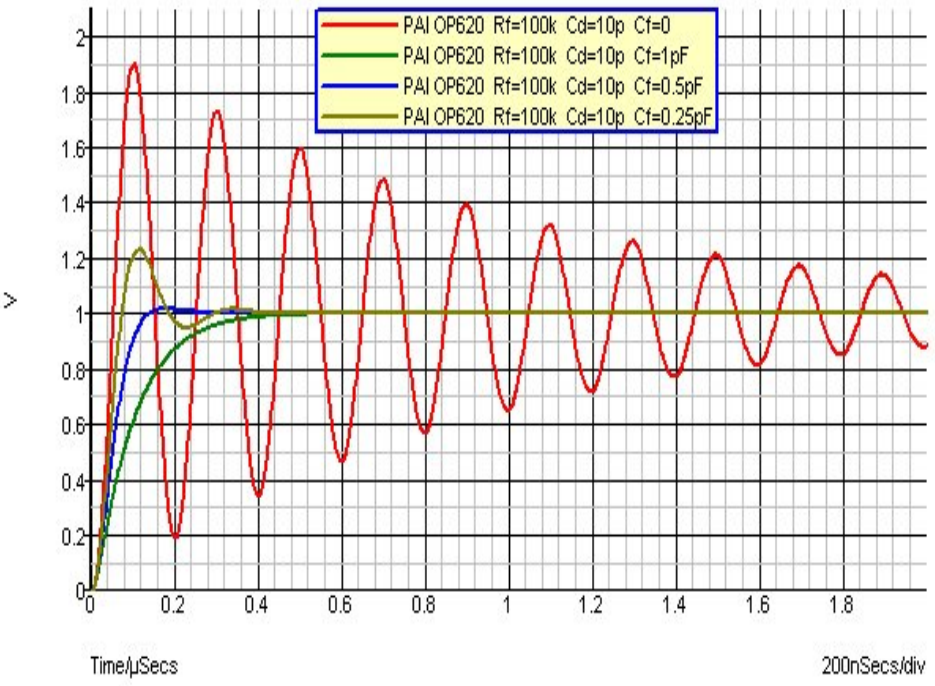
- **Transimpedance configuration**
  - $V_{out}(\omega)/i_{in}(\omega) = - R_f / (1+Z_f/GZ_d)$
  - Gain = R_f
  - High counting rate
  - Typically optical link receivers



Current sensitive preamp

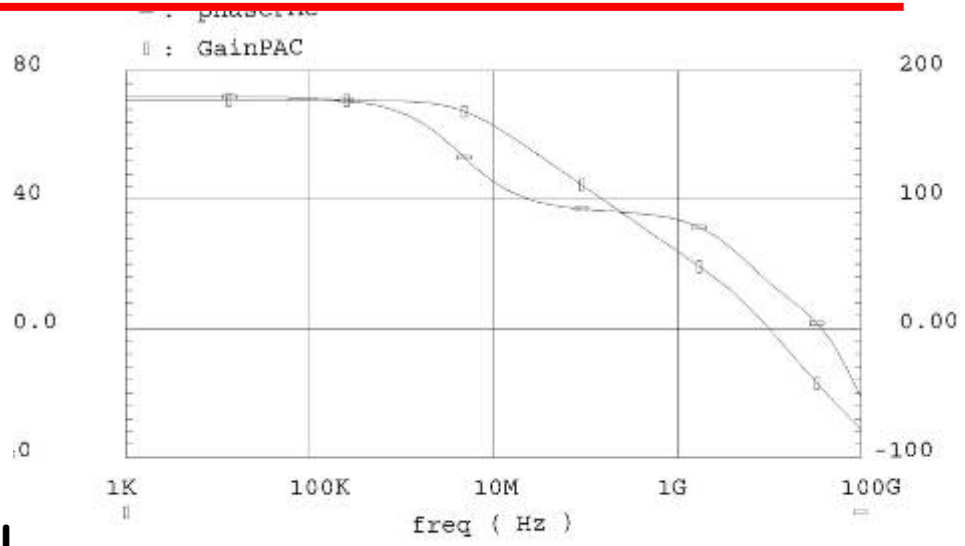
- **Easily oscillatory**
  - Unstable with capacitive detector
  - Inductive input impedance

    $L_{eq} = R_f / \omega_C$
  - Resonance at : $f_{res} = 1/2\pi \sqrt{L_{eq}C_d}$
  - Quality factor : $Q = R / \sqrt{L_{eq}/C_d}$
    - $Q > 1/2$ -> ringing
  - Damping with capacitance C_f
    - $C_f=2 \sqrt{(C_d/R_f G_0\omega_0)}$
    - Easier with fast amplifiers
    -



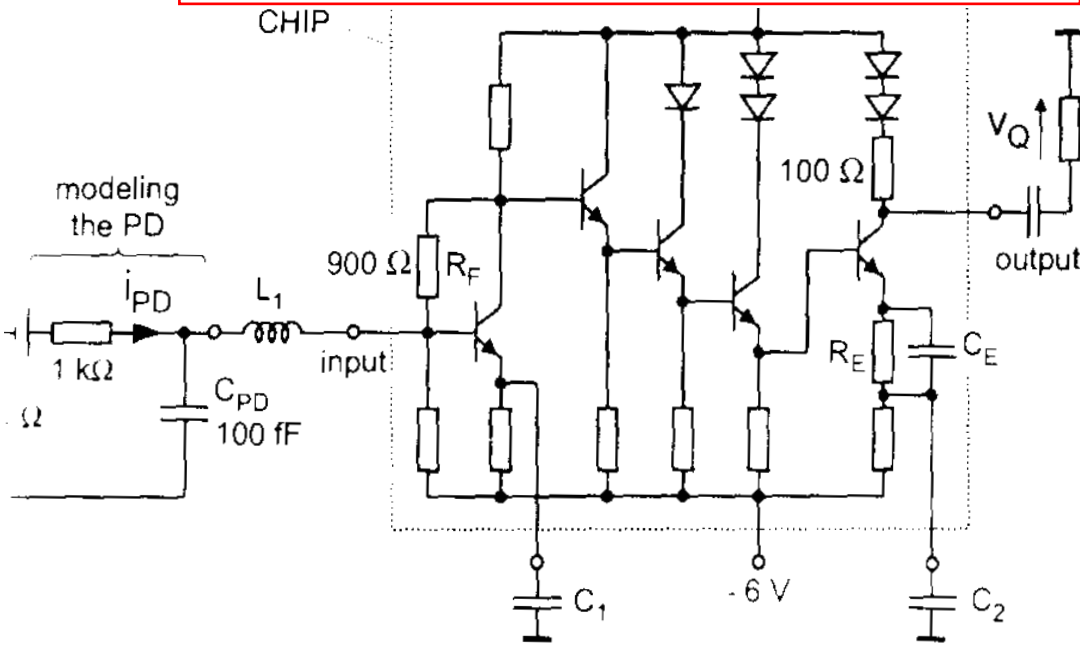
High speed transimpedance amplifier

- **Fast transimpedance amplifiers**
  - Rf= 25k Cf=10fF
  - SiGe process
  - 15 GHz gain-bandwidth product



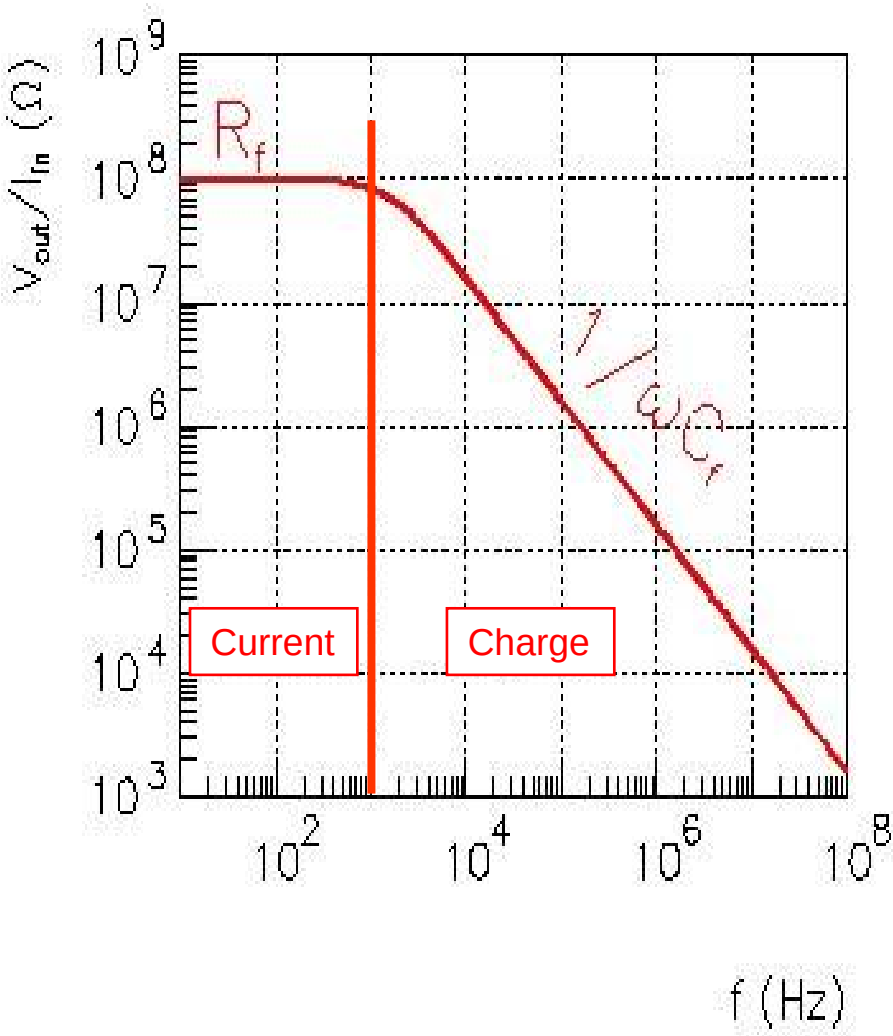
Open loop frequency response of SiGe amplifier

- **40 Gb/s transimpedance for optical**
  - Simple architecture (CE + CC)
  - SiGe bipolar transistors
  - CC outside feedback loop
  - « pole splitting »



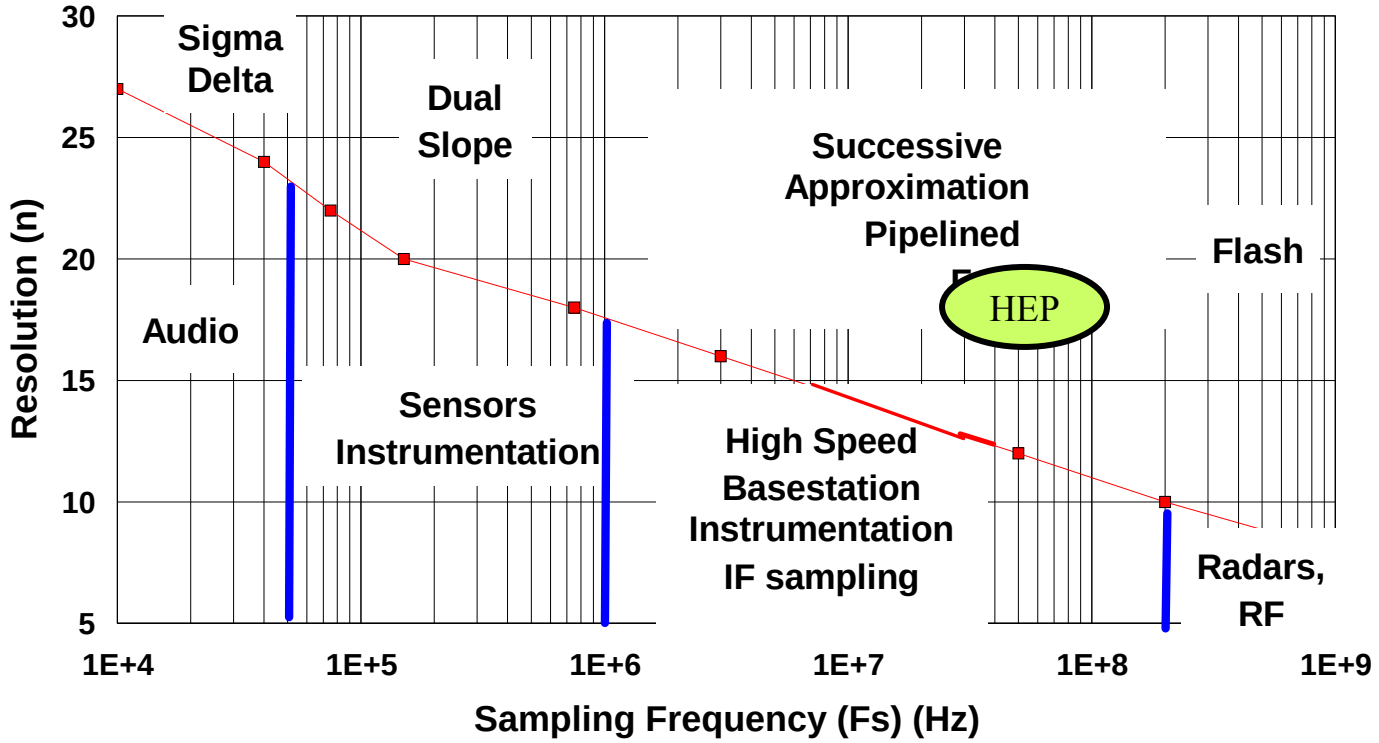
Charge vs Current preamps

- **Charge preamps**
  - Best noise performance
  - Best with short signals
  - Best with small capacitance
- **Current preamps**
  - Best for long signals
  - Best for high counting rate
  - Significant parallel noise
- **Charge preamps are not slow, they are long**
- **Current preamps are not faster, they are shorter (but easily unstable)**



ADCs : G.D.A.S.A.P.

- **The era of G.D.A.S.A.P. : « go digital as soon as possible »**
  - Spectacular evolution of ADCs : more bits, faster, less watts
  - Propelled by evolution of technologies and telecom
- **Has revolutionnized signal processing**
- **Now coming inside the ASICs**

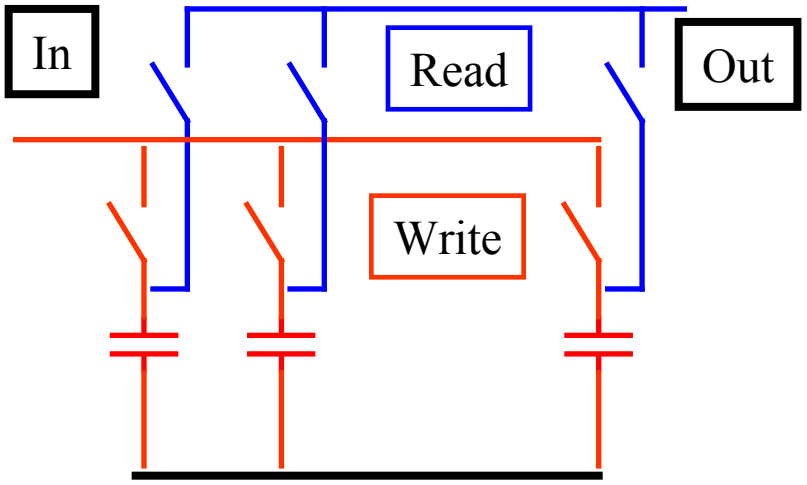


Resolution vs speed of ADCs in 2002

© L. Dugoujon STm

Analog memories

- **Switched Capacitor Arrays (SCAs)**
  - Store signal on capacitors (~pF)
  - Fast write (~ GHz)
  - Slower read (~10MHz)
  - Dynamic range : 10-13 bits
  - depth : 100-2000 caps
  - Unsensitive to cap absolute value (voltage write, voltage read)
  - Low power
  - Possible loss in signal integrity (droop, leakage current)

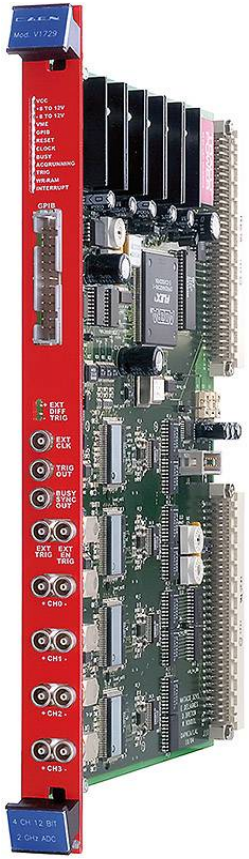


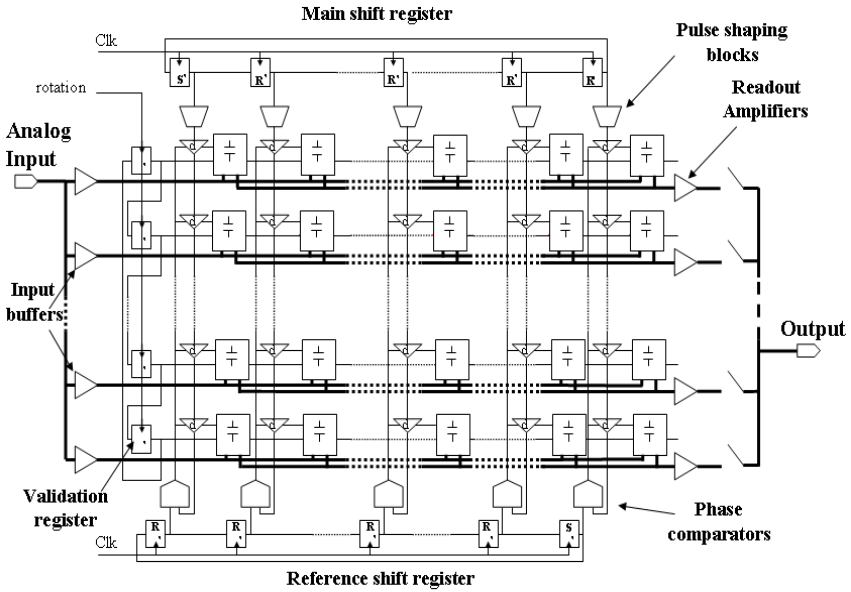
Principle of a « voltage-write, voltage-read » analog memory

- **The base of 90% of digital oscilloscopes !**

The MATACQ chip: an oscilloscope on a chip

- Based on the Sampling Matrix principle: evolution of the sampling DLL technique.
- Also includes 10ps precision TAC for trace synchronisation..
- AMS 0.8µm technology
- 2560 samples.
- < 1µs readout time.
- 50 MS/s-2GS/s range.
- 300 MHz Bandwidth.
- 13.5 bit rms dynamic range
- Jitter < 30 ps rms.





IEEE TNS 52-6:2853-2860,2005

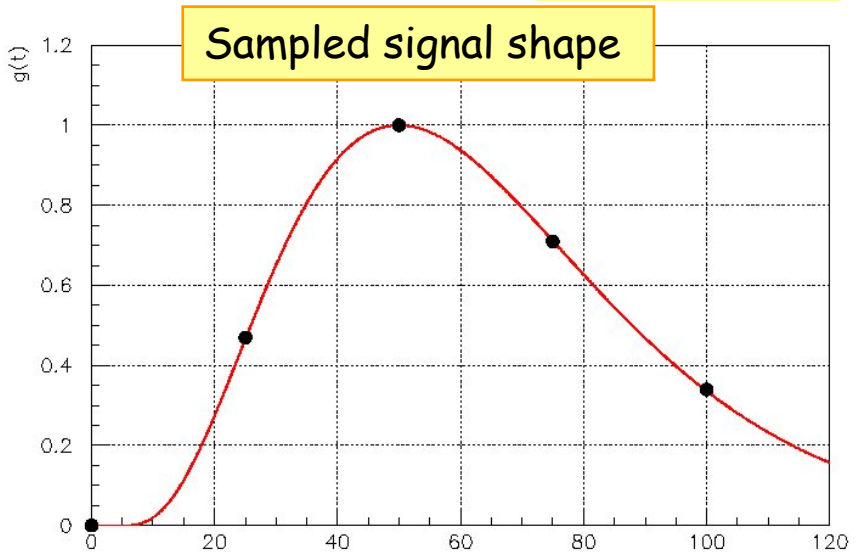
- used in the MATACQ (CAEN V1729) board.
- used to read fast photodetectors in small scale experiments or test benches

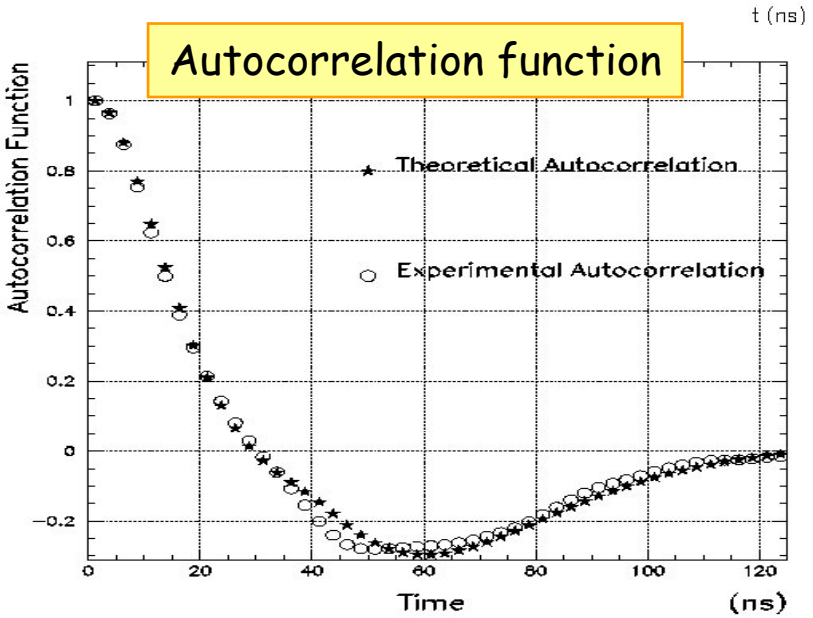
Digital filtering

- **Linear sums of sampled signal**
  - Finite Impulse Respopnse (FIR)
  - **made possible by fast ADCs (or analog memories)…**

- **Signal : s(t)=Ag(t)+b**
  - A : amplitude
  - G(t) : normalised signal shape
  - B : noise
  - Sampled signal : $s_i=Ag_i+b_i$

- **Filter : weighted sum $\Sigma\ a_i\ s_i$**
  - $a_i = \Sigma\ R^{-1}_{ij}\ g_i$
  - R = autocorrelation fonction
  - g_i = signal shape
    (0, 0.63, 1, 0.8, 0.47)
  - $S = \Sigma^{n}_{i=1}\ a_i s_i$



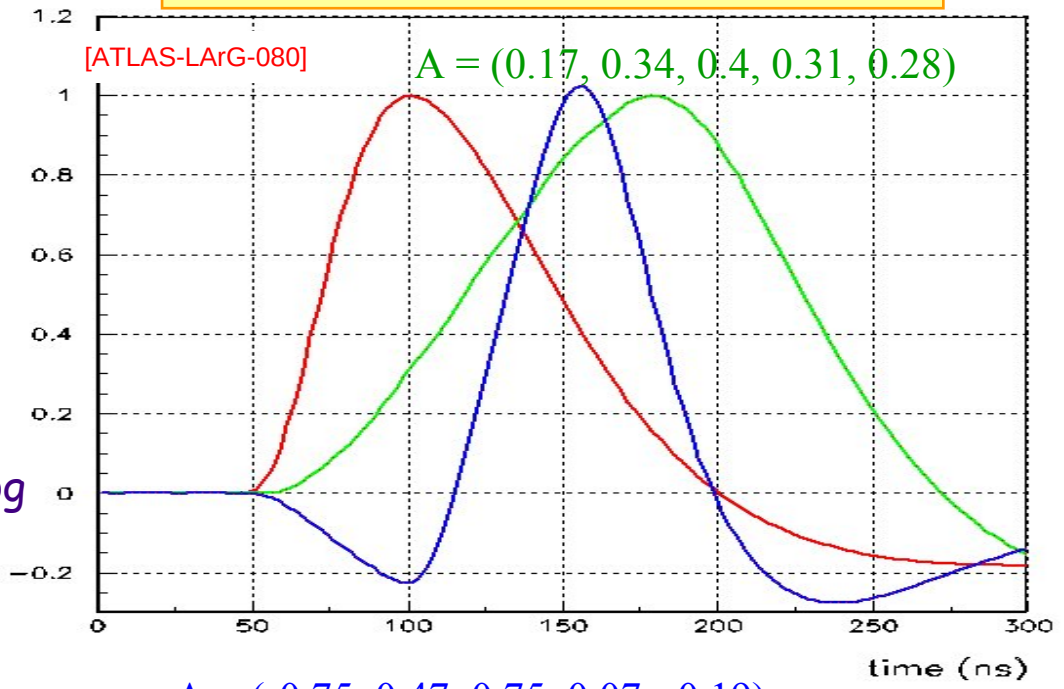


Exemple : ATLAS "multiple sampling"

©L. Serin (LAL)

- **Slowing down the signal**
  - Reduction of series noise
  - Similar to a simple integration
- **Accelererating the signal**
  - Reduction of pileup noise
  - Similar to a differentiation
- **Measuring the timing**
- **Some questions**
  - How does-it compare to an analog filter
  - How many samples are needed ?
  - What accuracy is needed on the waveform and on the autocorrelation ?
  - What analog shaping time is needed ?
  - Is the analog filter really useful ?

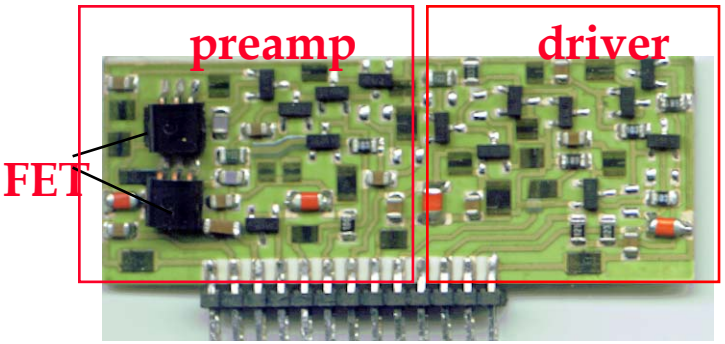
Signal before and after digital filtering



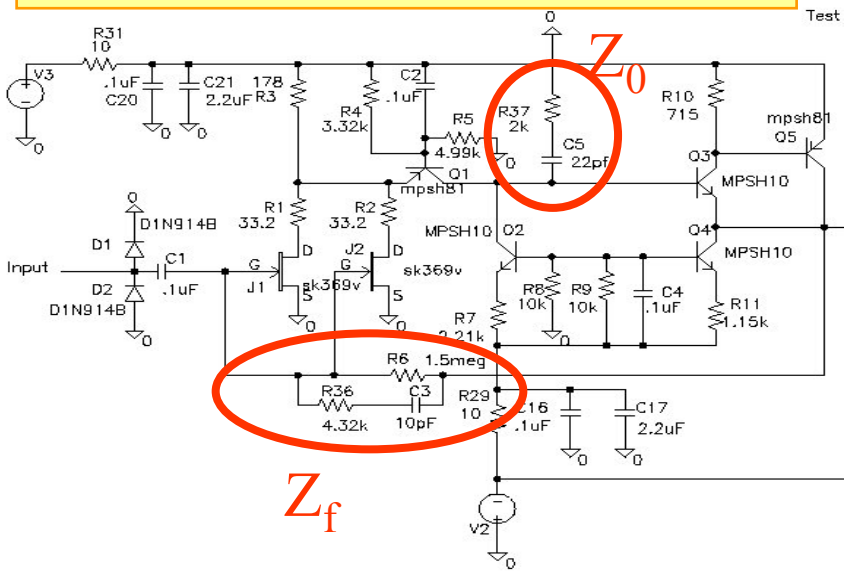
A = (-0.75, 0.47, 0.75, 0.07, -0.19)

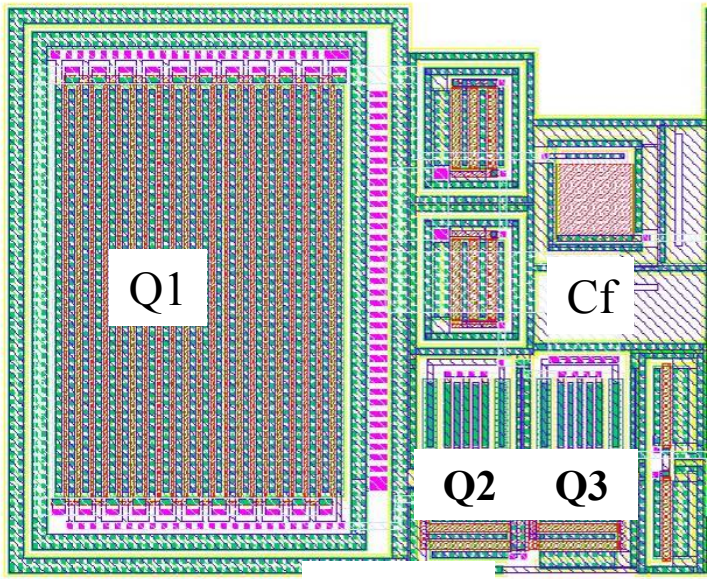
(R)evolution of analog electronics (1)

- **Acces to microelectronics**

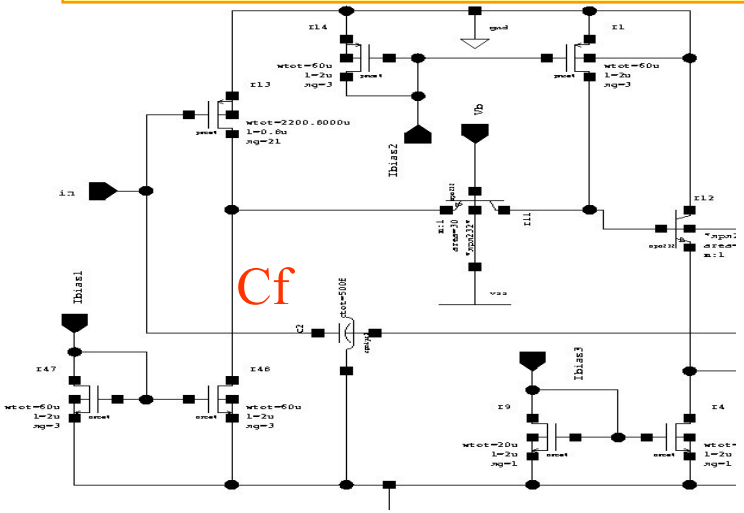


Charge preamp in SMC hybrid techno





Charge preamp in 0.8µm BiCMOS

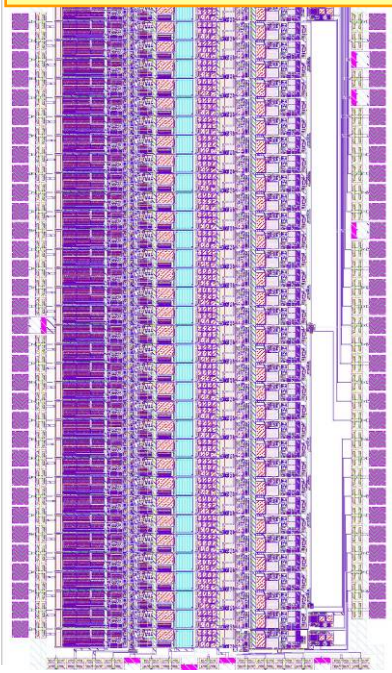


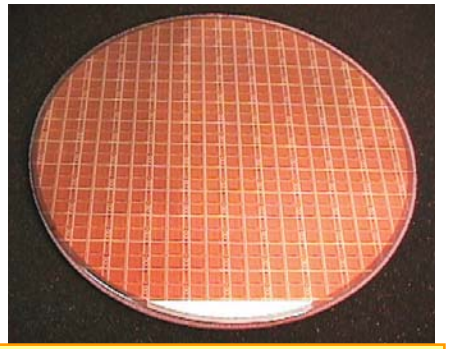
(R)evolution of analog electronics (2)

- **ASICs : Application Specific Integrated Circuits**
  - Access to foundries through multiproject runs (MPW)
  - Reduced development costs : 600-1000 €/mm^2 compared to dedicated runs (50-200 k€)
  - Full custom layout, at transistor level
  - mostly CMOS & BiCMOS

- **Very widespread in high Energy Physics**
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better performance : reduction of parasitics
  - Better reliability (less connections)
  - But longer developpement time

Layout 32ch ASIC

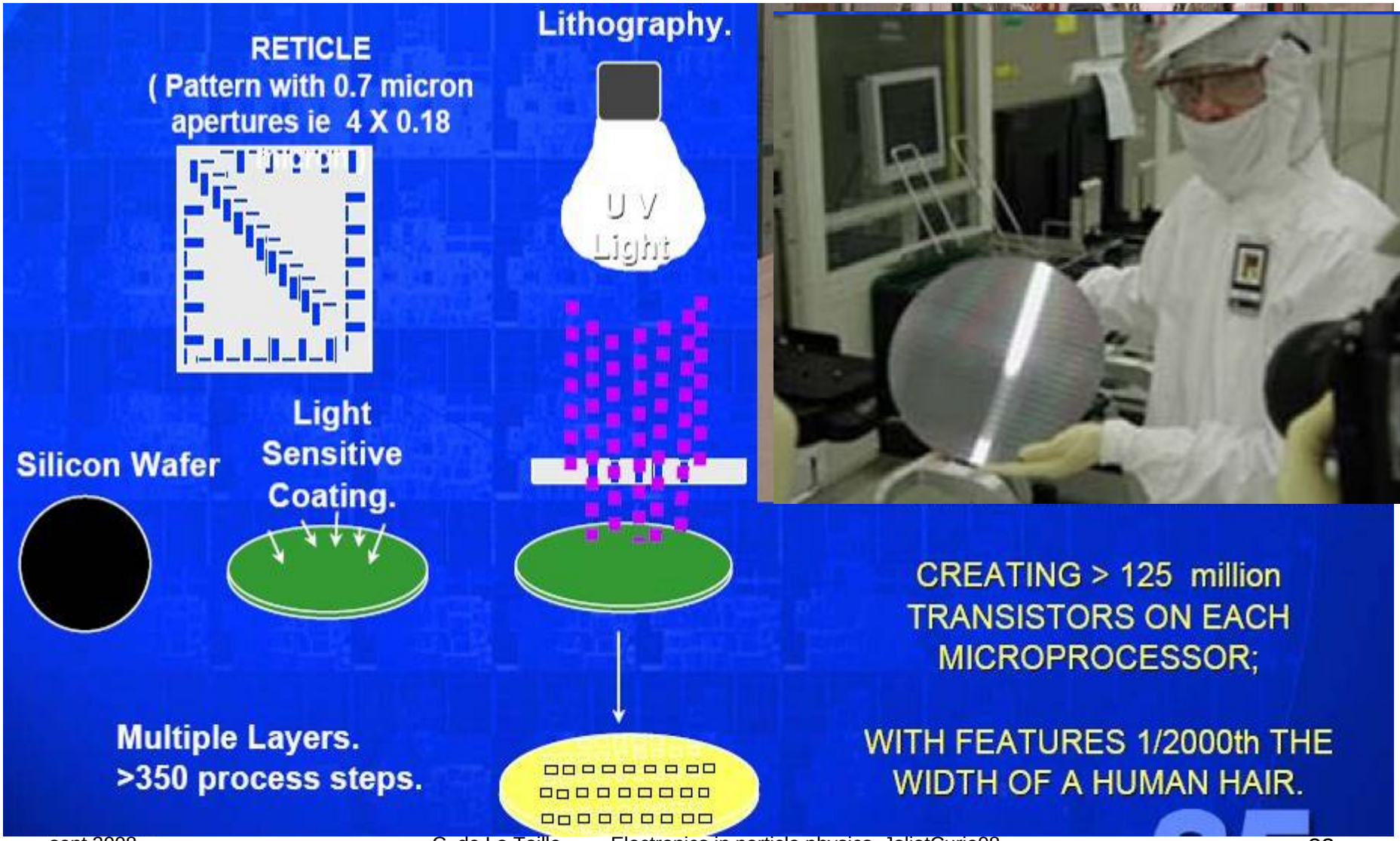




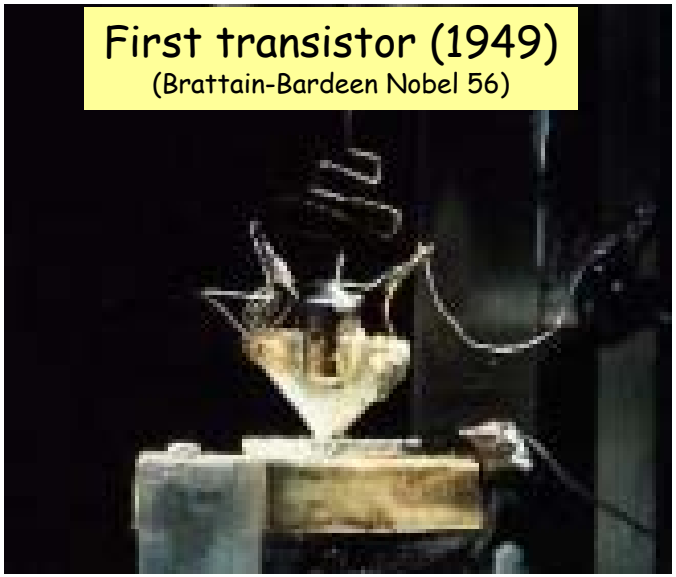
300 mm wafer (IBM)

Processing of ASICs

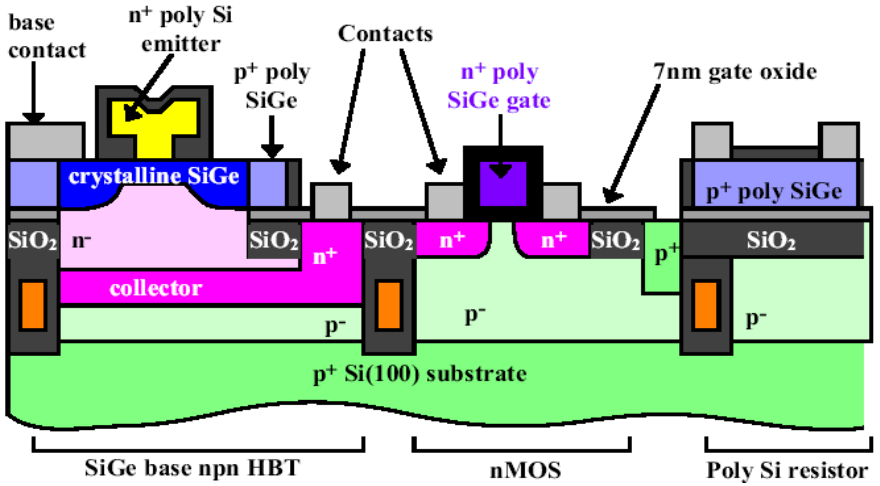
- From Sand to ICs…



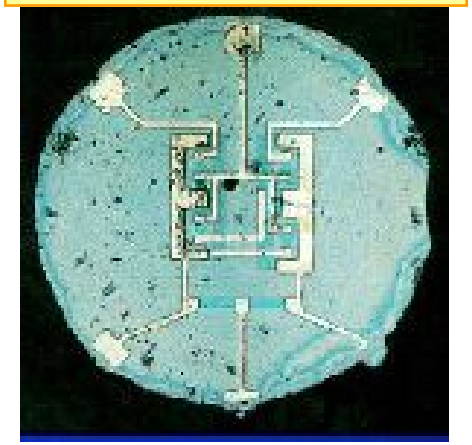
Evolution of technologies



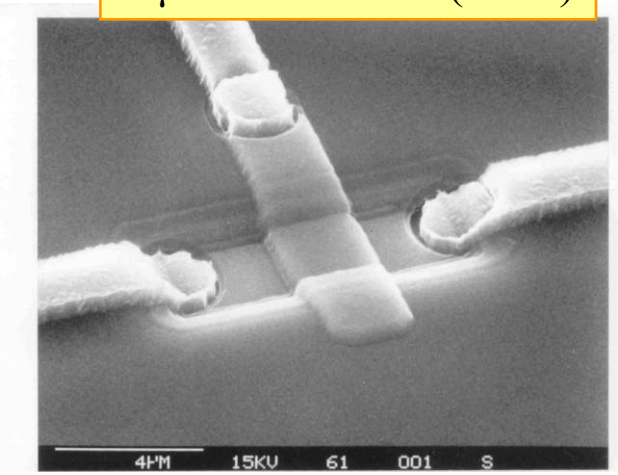
SiGe Bipolar in 0.35µm monolithic process



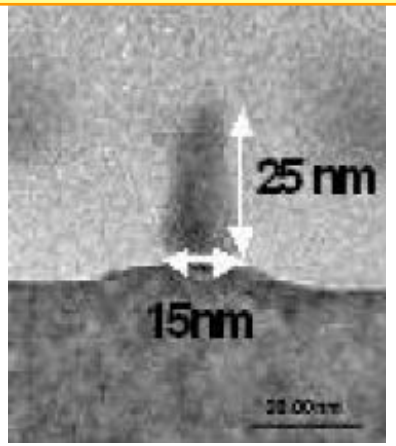
First planar IC (1961)



5 µm MOSFET (1985)

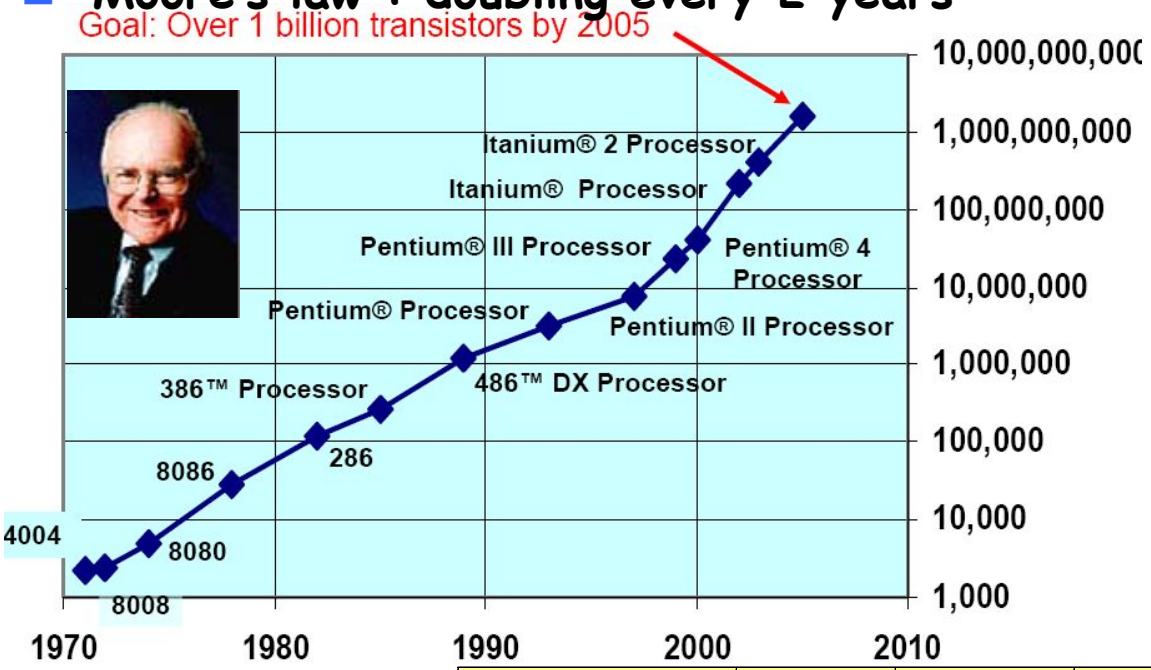


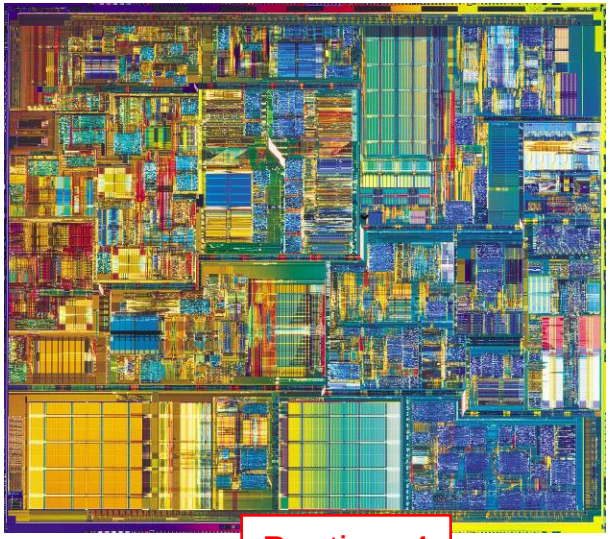
15 nm MOSFET (2005)



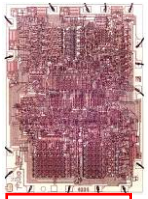
Evolution of CMOS technologies

- **Moore's law : doubling every 2 years**





Pentium 4

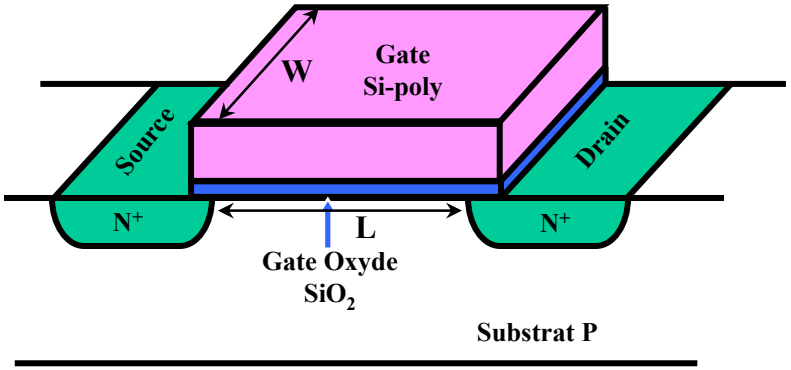


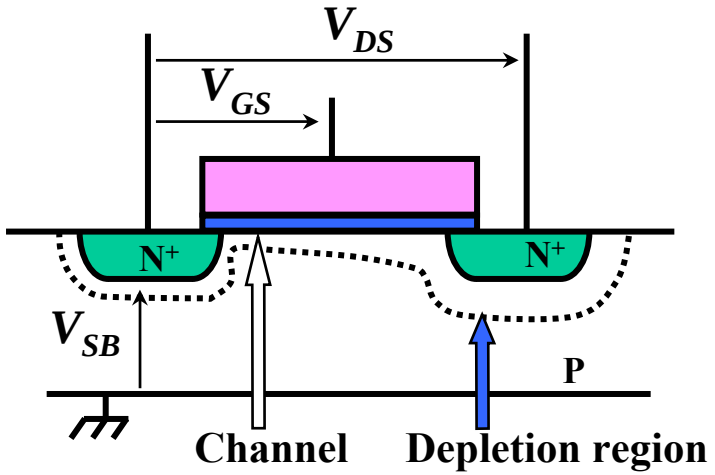
4004

Microprocesseur	4004	8086	i386	Pentium	Pentium 4
Année	1971	1978	1985	1993	2000
Nb. Bits	4	16	32	64	64
Horloge (Hz)	108k	10M	33M	66M	1.5G
Mémoire adressable (bytes)	640	1M	16M	4G	64G
Technologie (µm)	10	3	1	0.8	0.18
Nb transistors	2300	29000	275000	3.1M	42M
Tension alim (V)	12	5	5	5/3.3	1.3 interne

« CMOS scaling »

- **Reduction of dimensions**
  - Gate length : L
  - Oxide thickness : t_{ox}
- **Reduction of power supplies**
  - Reduction of power dissipation
- **Improvement of speed in $1/L^2$**
  - Transconductance : g_m a W/L
  - Capacitance : C a WL
  - speed : $F_T = g_m/C$ a $1/L^2$
- **Reduction of costs (?)**
  - Increase of integration density
- **Radiation hardness in bonus !**
  - Less trapping in gaye oxide

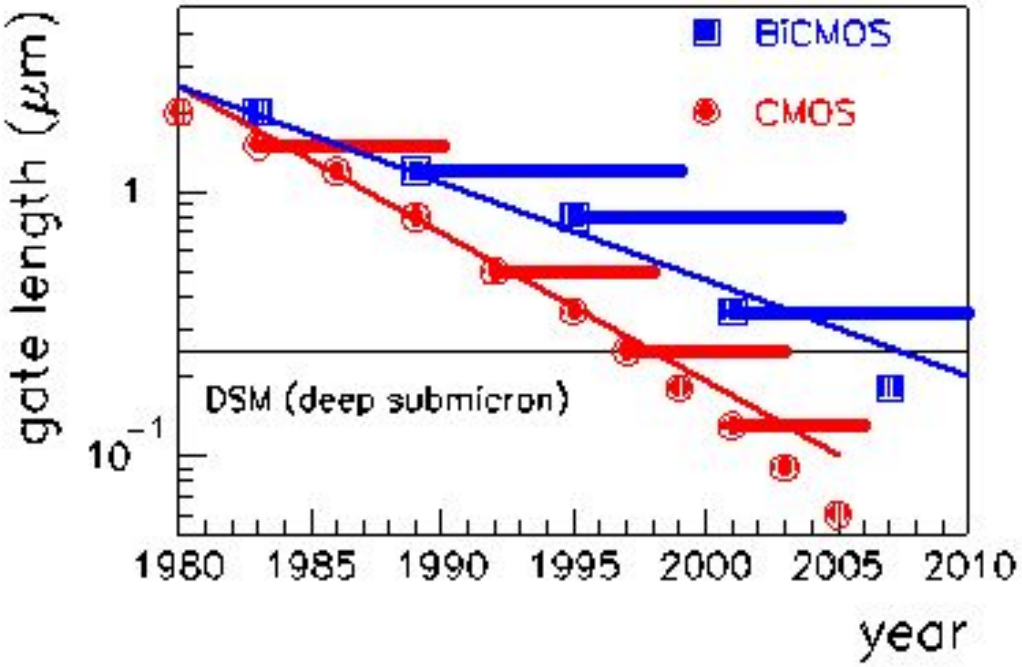


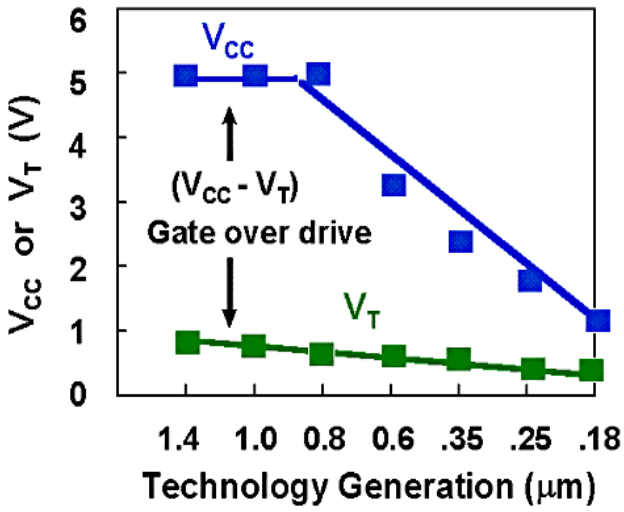


Principle of Nchannel MOSFET

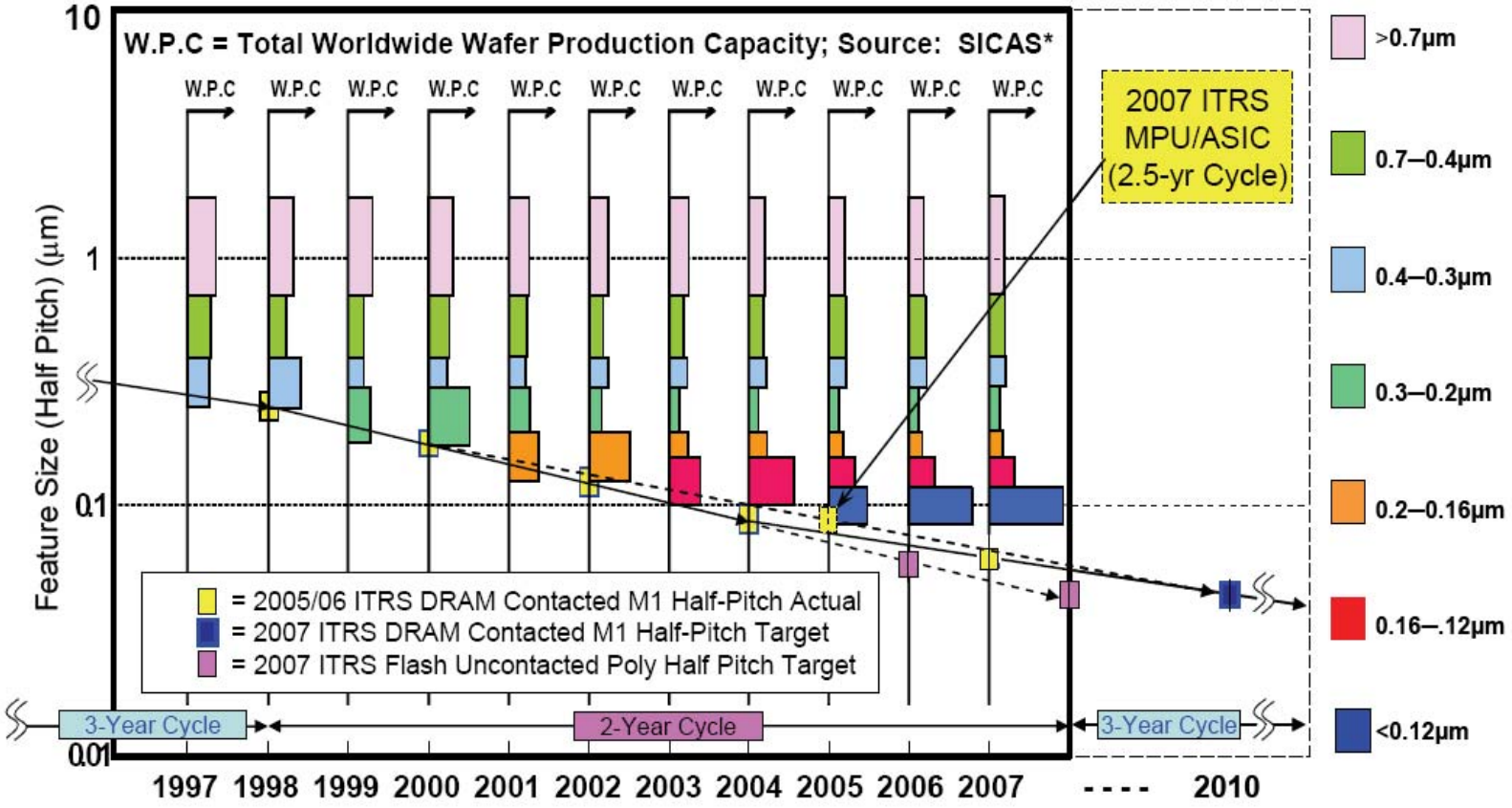
Evolution of CMOS technologies (2)

- **Differences between analog/mixed signall and digital technologies**
  - Very fast evolution of digital technologies (faster design migration)
  - More « perene » analog technologies (SiGe, BiCMOS…) (driven by mobile telecom and automotive)
  - A visible split occuring
- **More difficult analog design in low voltage**
  - « no more headroom for signals »



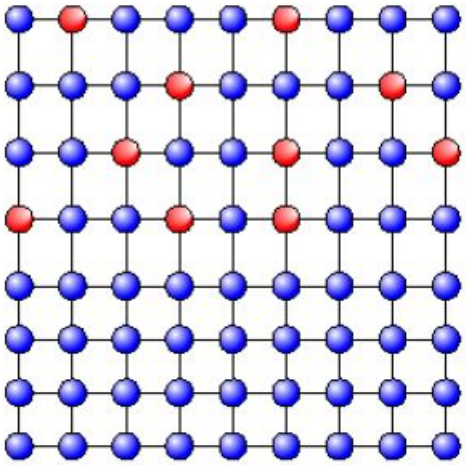


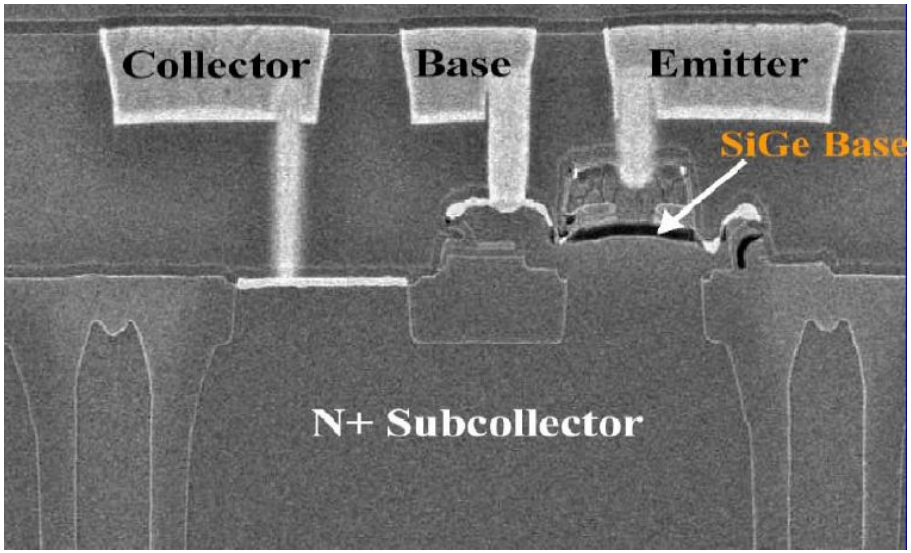
Semiconductor Industry Roadmap

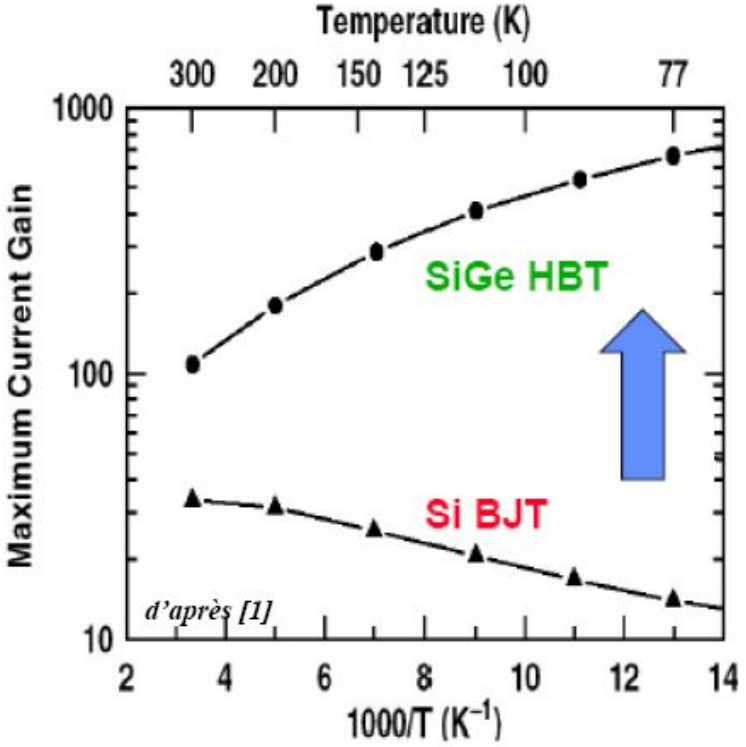


SiGe technology

- **Faster bipolar transistors for RF telecom**
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-signal design

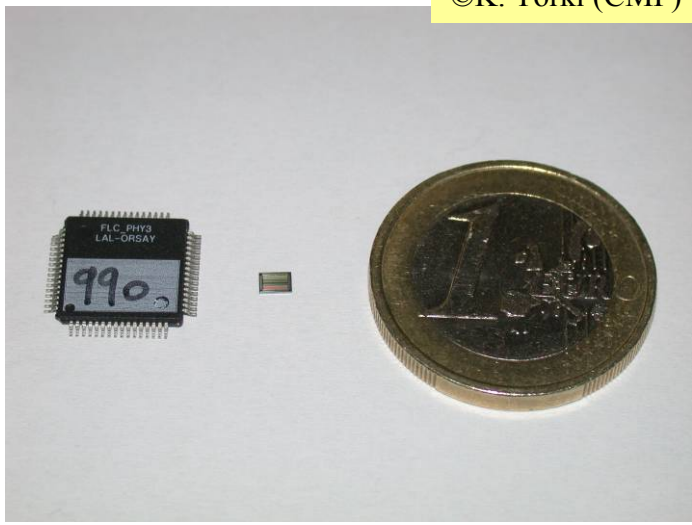






Cost of ASICs

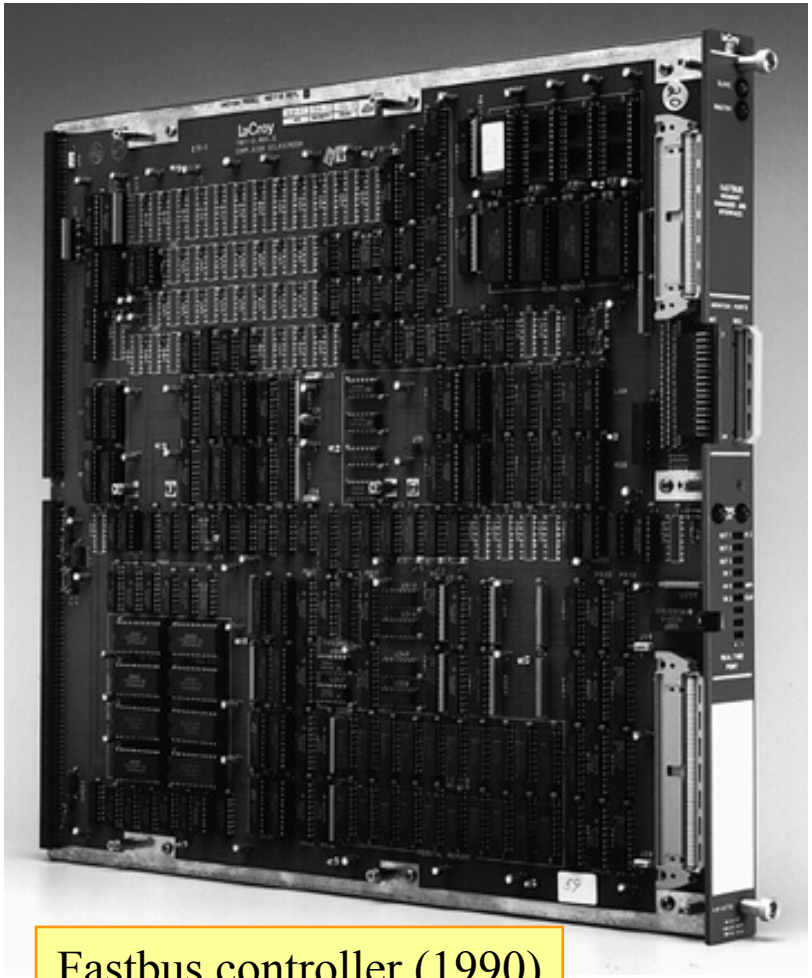
©K. Torki (CMP)



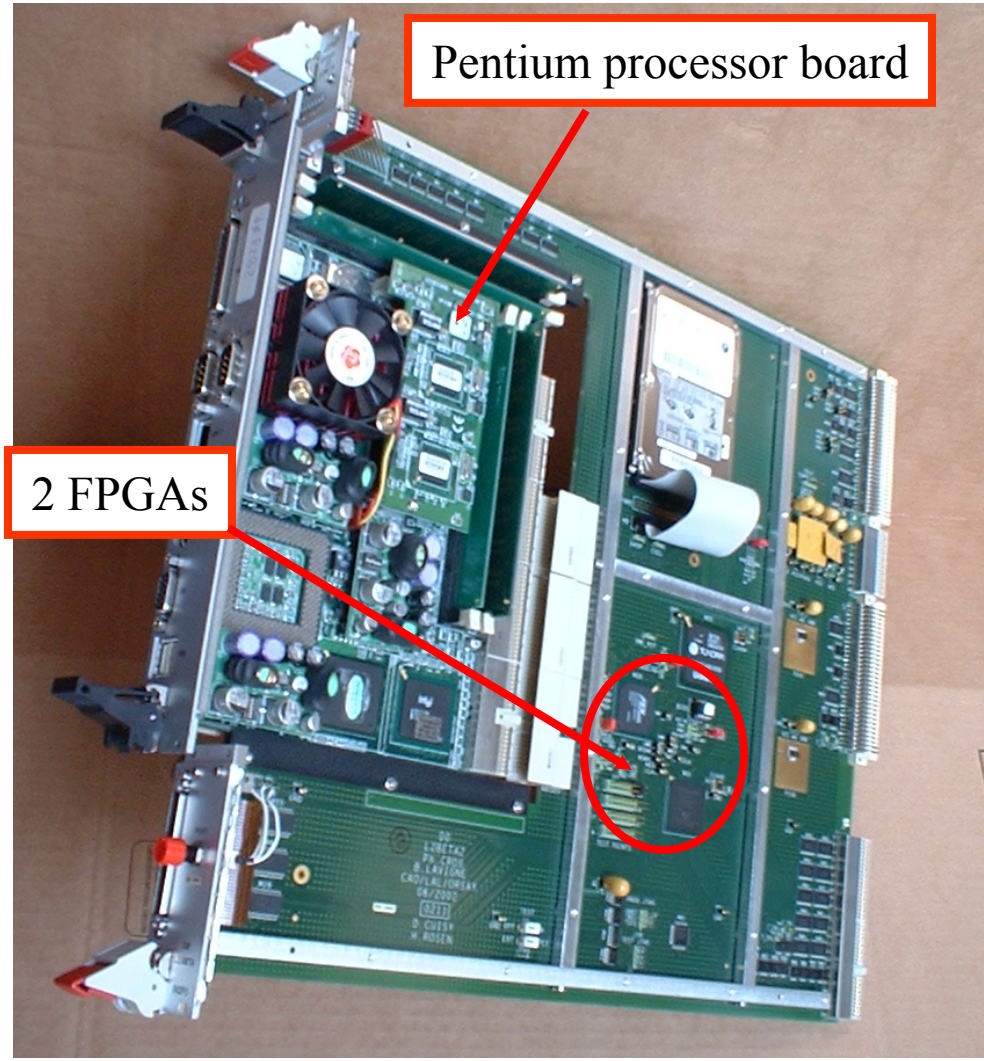
- **MPW (multi-project wafers)**
  - CMOS 0.35µm (AMS) : 650 €/mm2
  - BiCMOS SiGe 0.35 µm (AMS) : 900 €/mm2
  - CMOS 0.13µ (STm) : 2500 €/mm2
  - CMOS 90 nm (STm) : 5000 €/mm2
  - Usually a few 10 to 100 pieces in a MPW run
- **Production runs**
  - Masks : 91 k€ (CMOS 0.35µm)
  - 8" wafers : 4 k€, useful area : 25 000 mm2 = several thousands of chips
- **Packaging**
  - Ceramic : 20-30€/chip
  - Plastic : 2k€ + 1-2 €/chip
- **Example : chip 10mm2 16 channels**
  - 100 chips (MPW) : 120€/chip, 7€/channel
  - 10 000 chips (4wafers) : 12€/chip < 1€/channel

(R)evolution of digital electronics (1)

- From stacks of circuits to FPGAs : progammable gate arrays

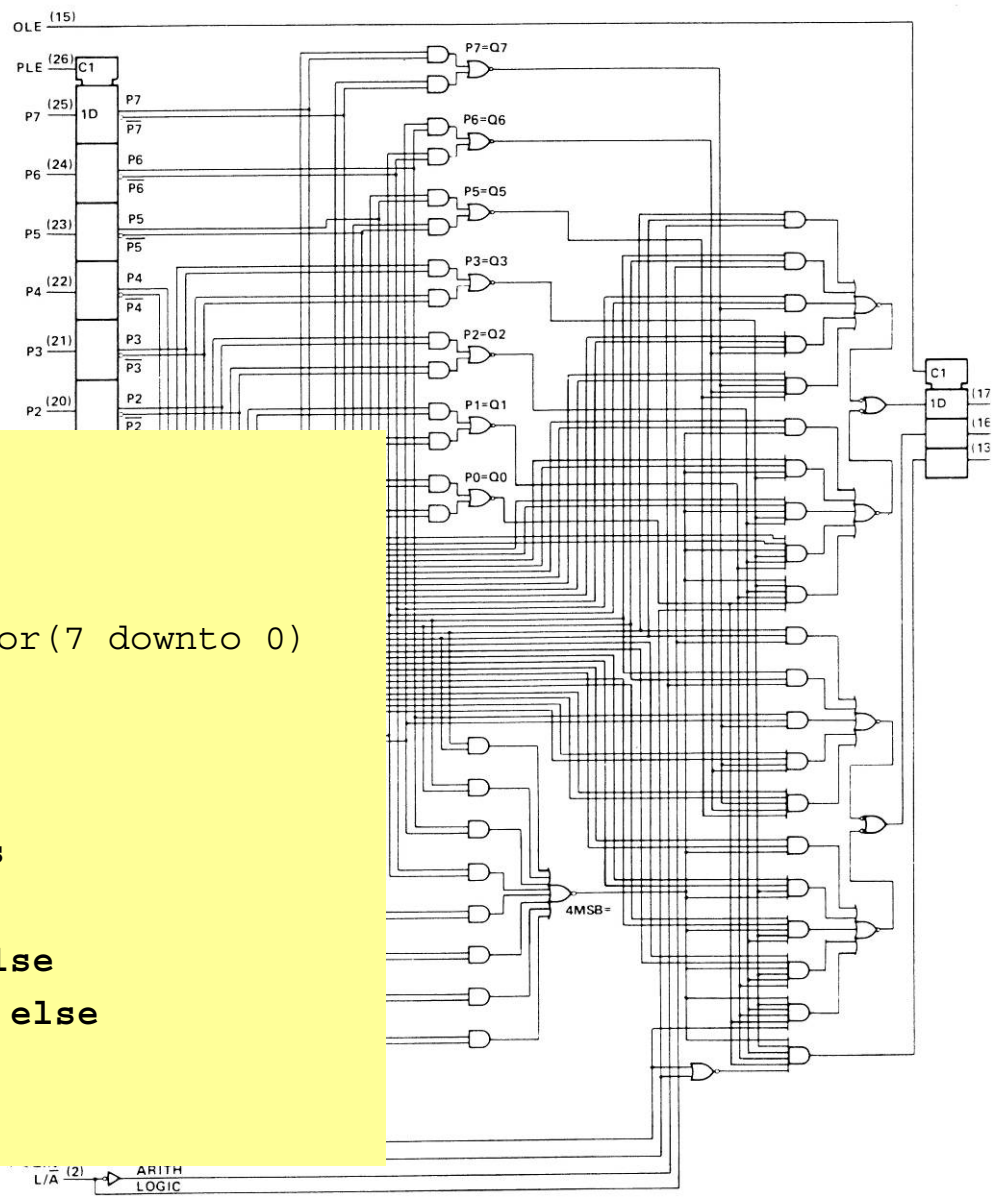


Fastbus controller (1990)



(R)evolution of digital electronics (2)

- **Schematic -> High level languages (Verilog, VHDL)**
  - Example 8 bit comparator
  - 74LS866



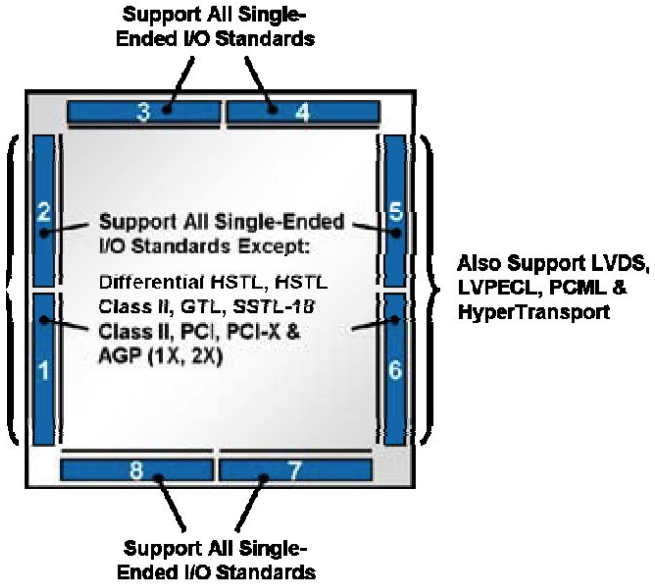
- **VHDL comparator :**

```
entity comparator_8 is
port (   raz : in std_logic;
         val1,val2 : in std_logic_vector(7 downto 0)
         result : out std_logic
       );
end entity comparator_8;
architecure archi_& of comparator_8 is
begin
   result <=      '0' when raz = '0' else
                  '1' when val1 > val2 else
                  '0'
end architecture archi_1;
```

(R)evolution of digital electronics (3)

- **Reduction of digital logic levels**
  - 1980 : TTL : 0-5 V
  - 2000 : LVDS : Low Voltage (± 400 mV) Differential Swing
  - Better signal integrity (EMC)
  - Reduction of power supplies 5V -> 3.3V -> 2.5V -> 1.2V

- **Components : the revolution of FPGAs :**
  - = Field Programmable Arrays (Altera©, Xilinx©)
  - 4-40 millions gates (55M in a Pentium4)
  - RISC 32bits processors
  - 10 Mbits resident memory
  - 2000 pins 1300 I/O (inputs/outputs)
  - 300 MHz operation



FPGAs as blackhole of digital electronics ?

RISC processors

IP standard interfaces (Ethernet, USB,PCI..)

Matching networks

DSP blocks, arithmetics

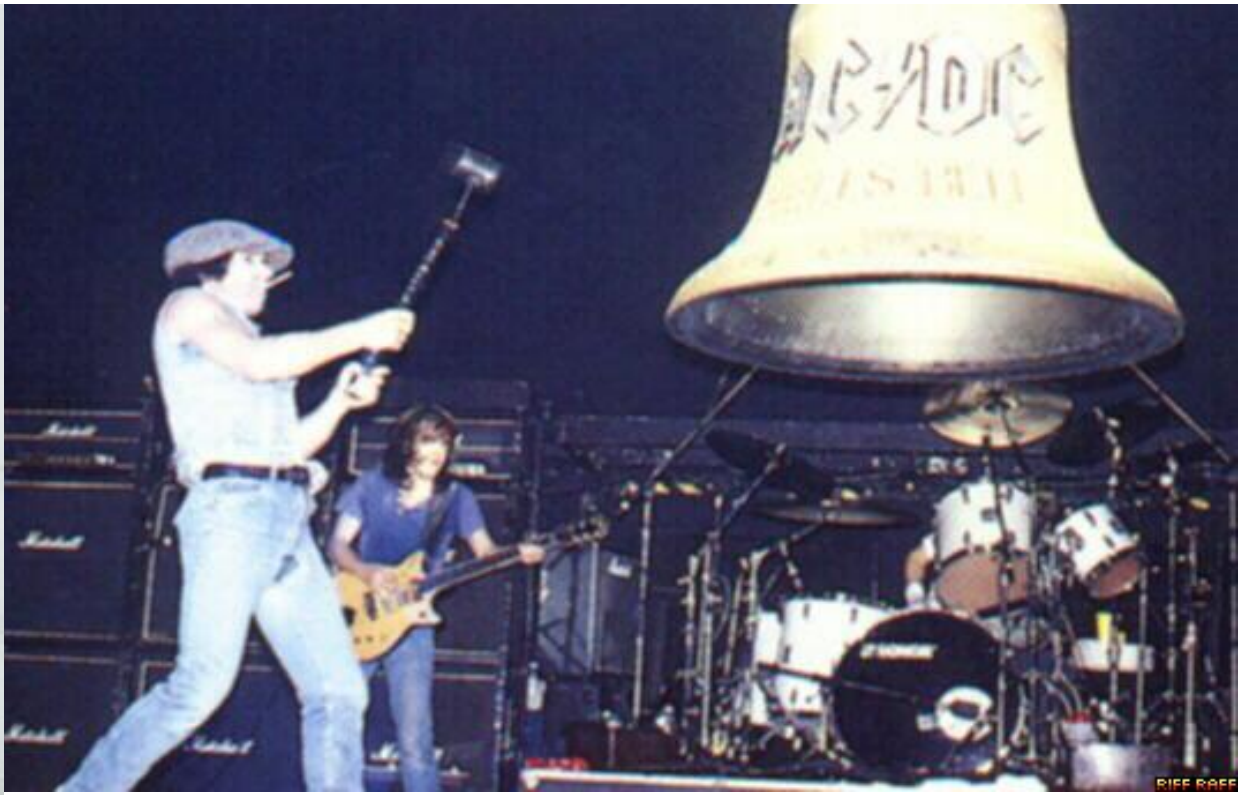
Clocks & PLLs

Memories & FIFOs

Bus interfaces (GTL, LVDS…)

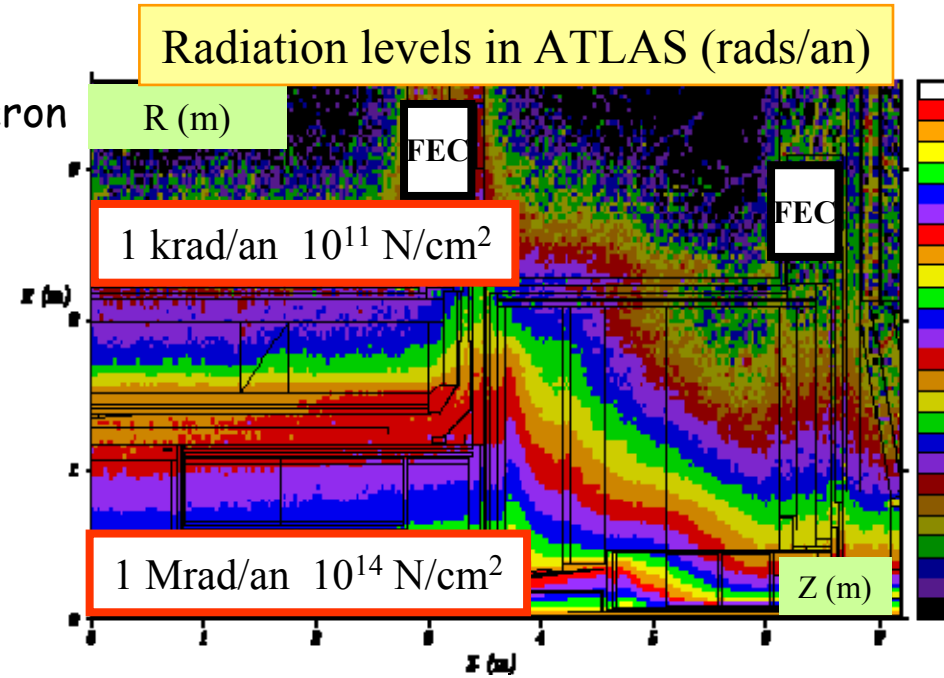
Electromagnetic compatibility (EMC-EMI)

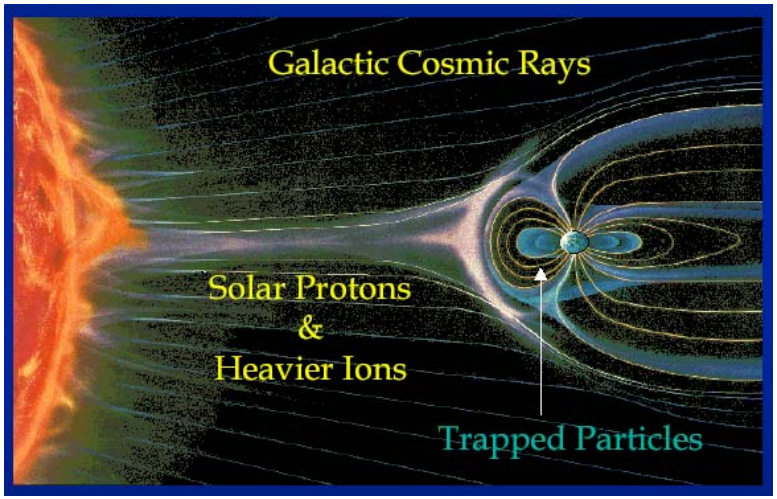
- **Coexistence analog-digital**
  - Capacitive, inductive and common-impedance couplings
  - A full lecture !
  - A good summary : there is no such thing as « ground », pay attention to current return



Effect of radiations on components

- **TID : total ionising dose effects**
  - Charge trapping in gate oxide
  - Alleviated in thin oxides (Deep SubMicron DSM)
  - Radiation tolerant layout techniques designed by CERN RD49 in 0.25µm
- **NIEL : non ionising energy loss**
  - Cristal damage with neutrons
  - Beta drop in bipolar transistors
- **SEU : Single Event Effect**
  - Effect of large ionising impact : local charge deposition on critical nodes
  - SEU : single event Upset = bit flip
  - SEL : single Event Latchup : thyristor setting -> destructive !





Radiation hardness : space vs LHC

	Space missions	LHC experiments
Mission Time	10-15 years	10 years
Service	Not Possible	Impractical
Electronics Reliability	High	High
Total Dose Requirements	10 -100 krad	1 krad - 10 Mrad
Non Ionizing Energy Loss (N)	~0	10^{13}-10^{15} N/cm2
Single Event Upsets	IC's SEU characterised No Critical SEU Accepted	

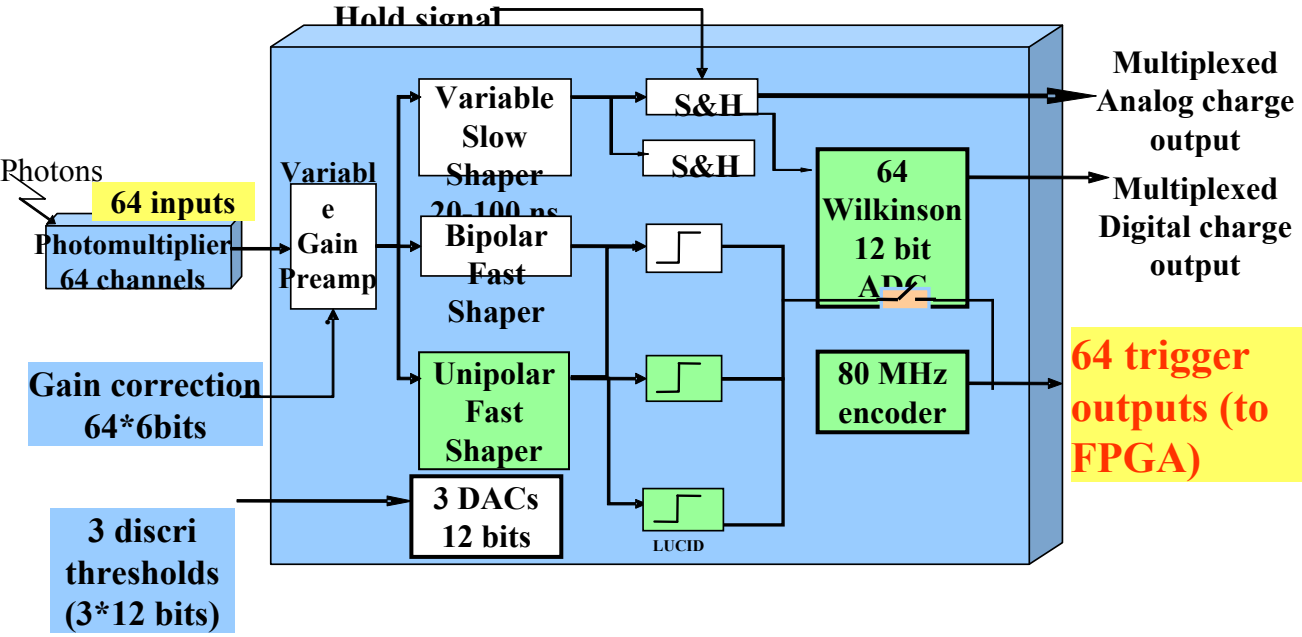
- => Similar requirements

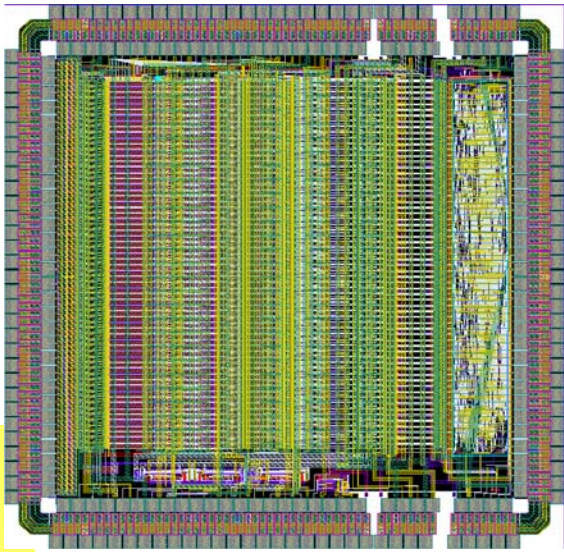
Examples and trends

- More pixels => more integration
- System on chip => more integration !
- 3D integration : still more integration !

MAROC : 64 ch MAPMT chip for ATLAS lumi

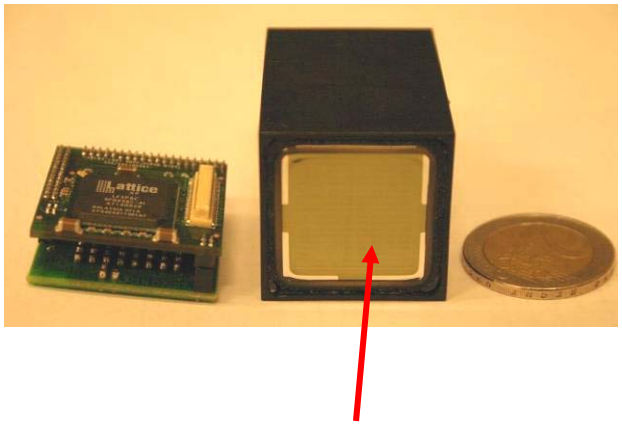
- **Complete front-end chip for 64 channels multi-anode photomultipliers**
  - Auto-trigger on 1/3 p.e. at 10 MHz, 12 bit charge output
  - SiGe 0.35 µm, 12 mm2, Pd = 350mW



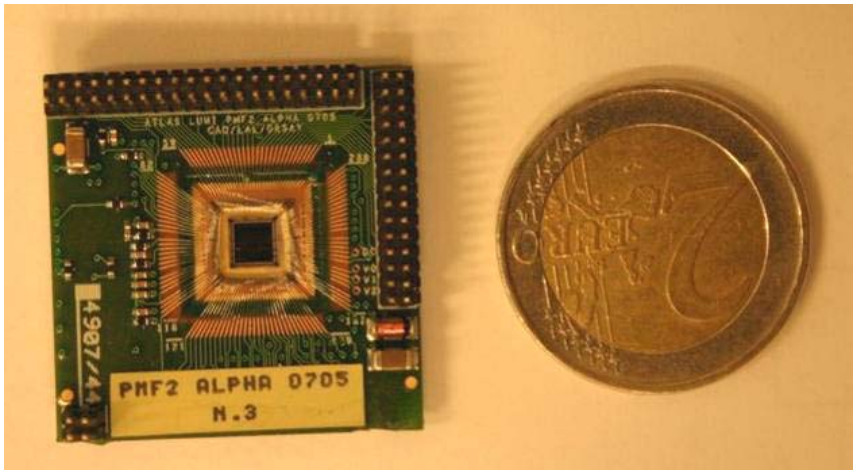


Active board pictures

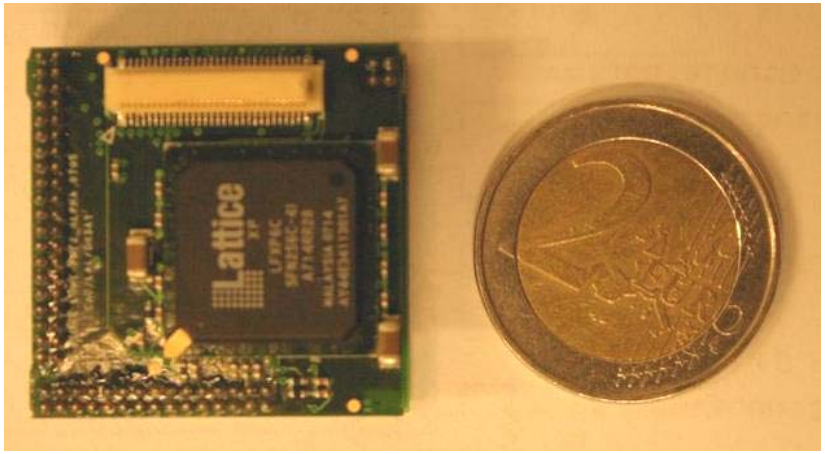
MAROC2 chip bounded at CERN



64 ch PMT

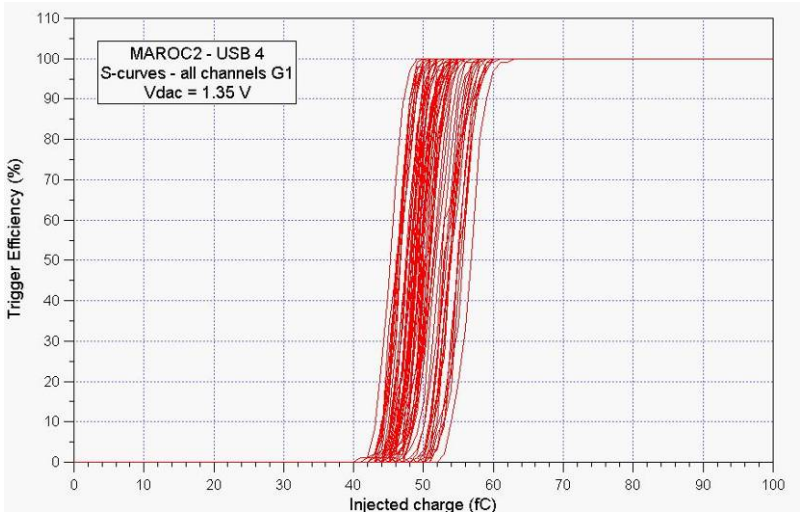


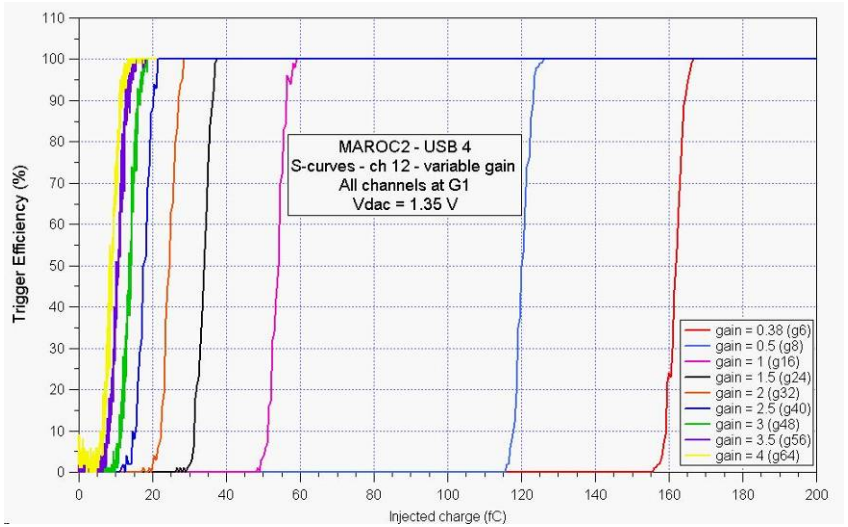
MAROC side

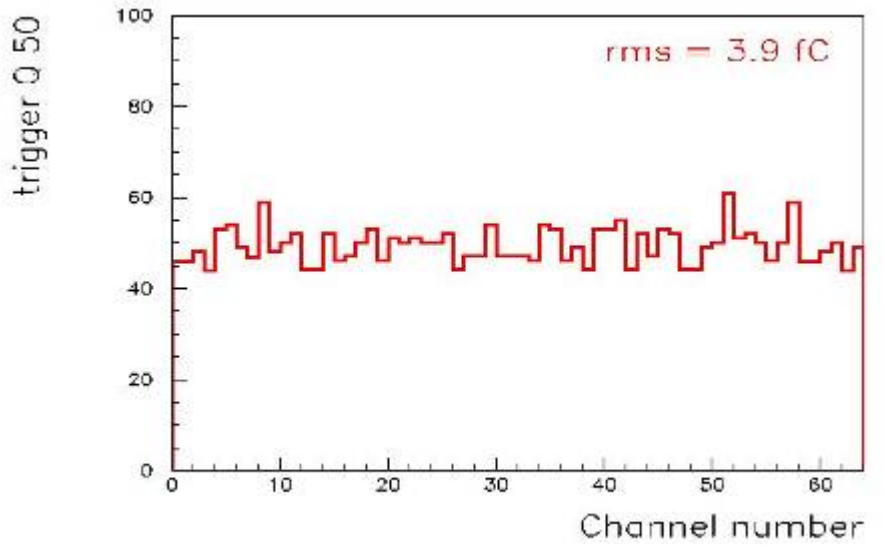


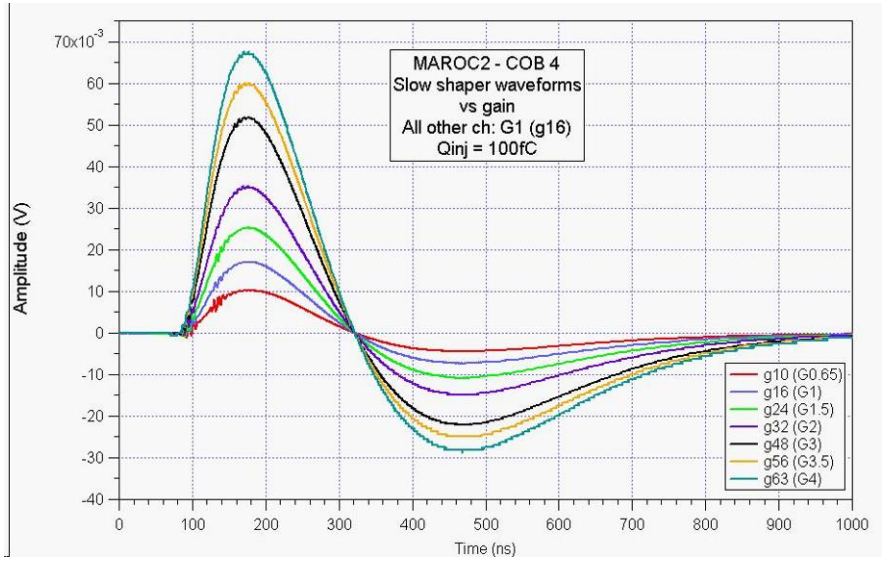
Lattice side

MAROC Efficiency curves

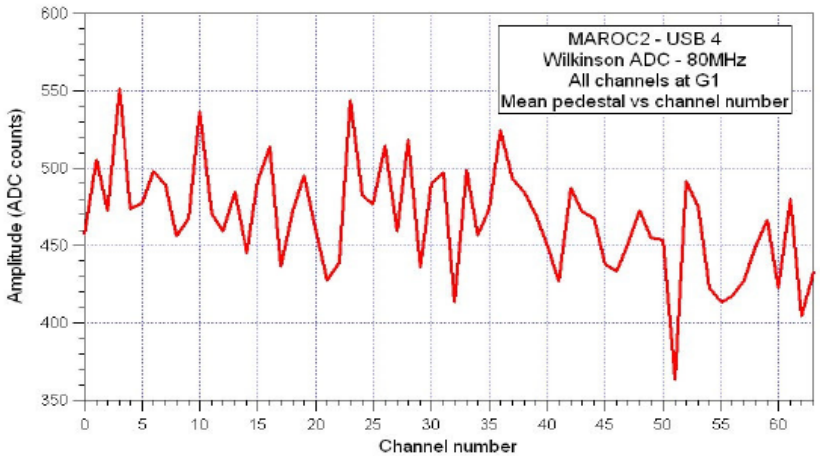


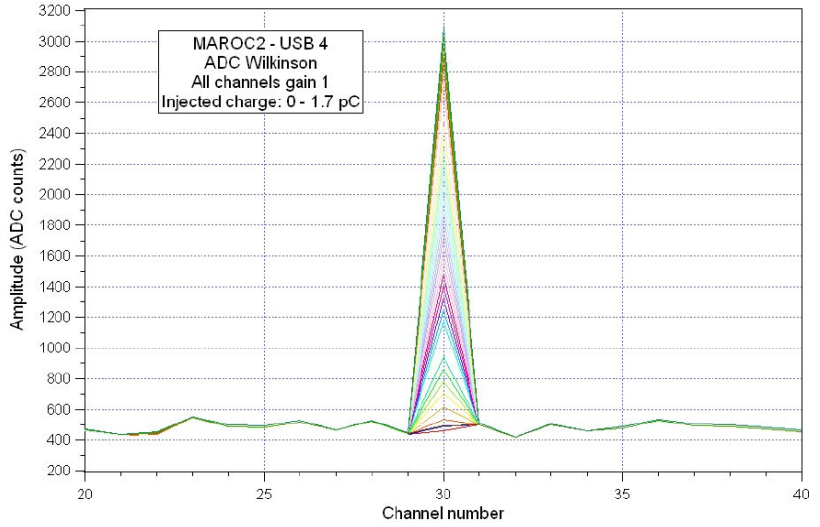




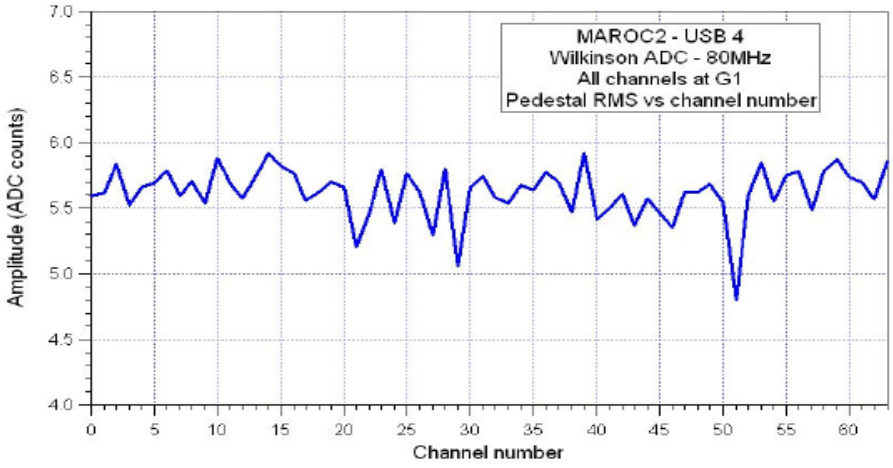


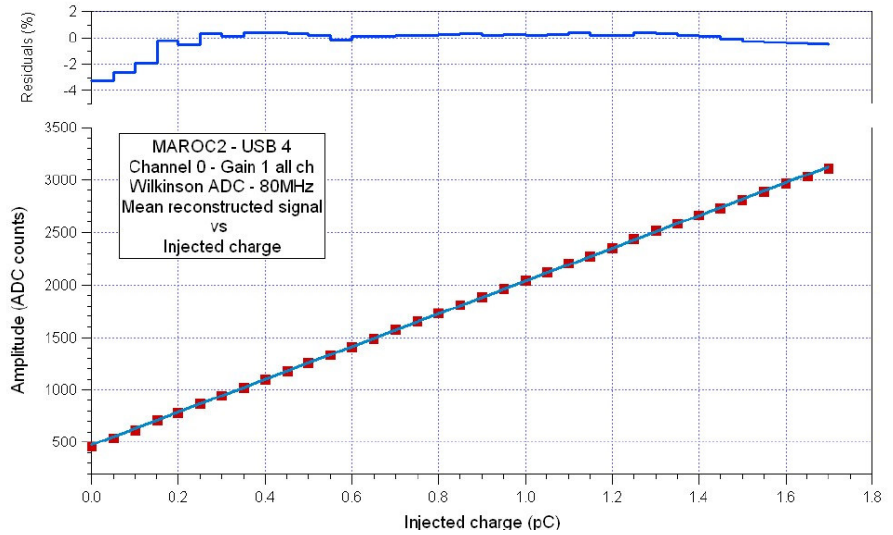
MAROC 2: Charge output Wilkinson ADC





INTERNAL ADC

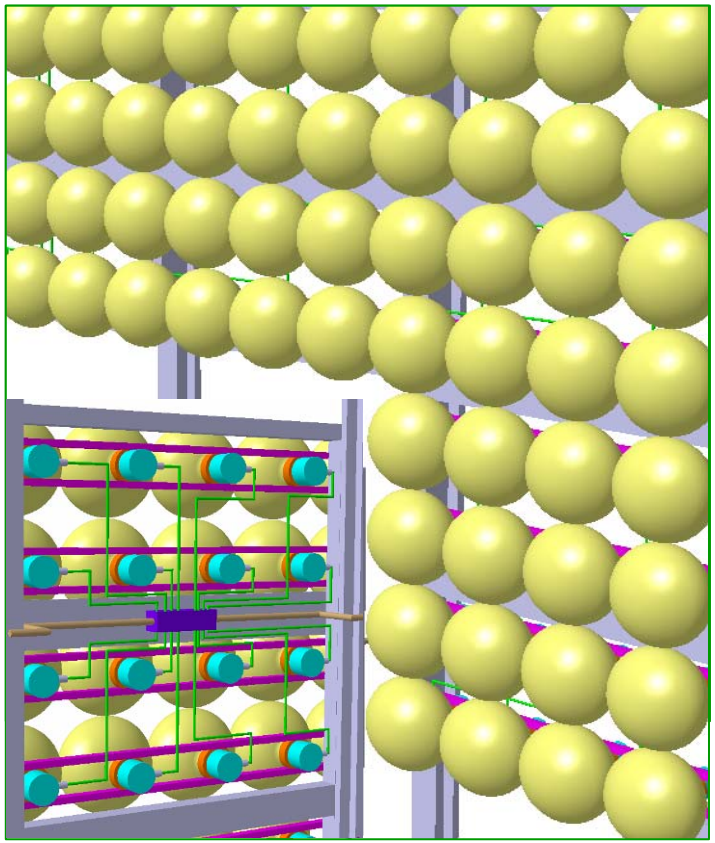




- **Measurements performed with the internal Wilkinson ADC**
- **Linearity of ± 2% approximately**

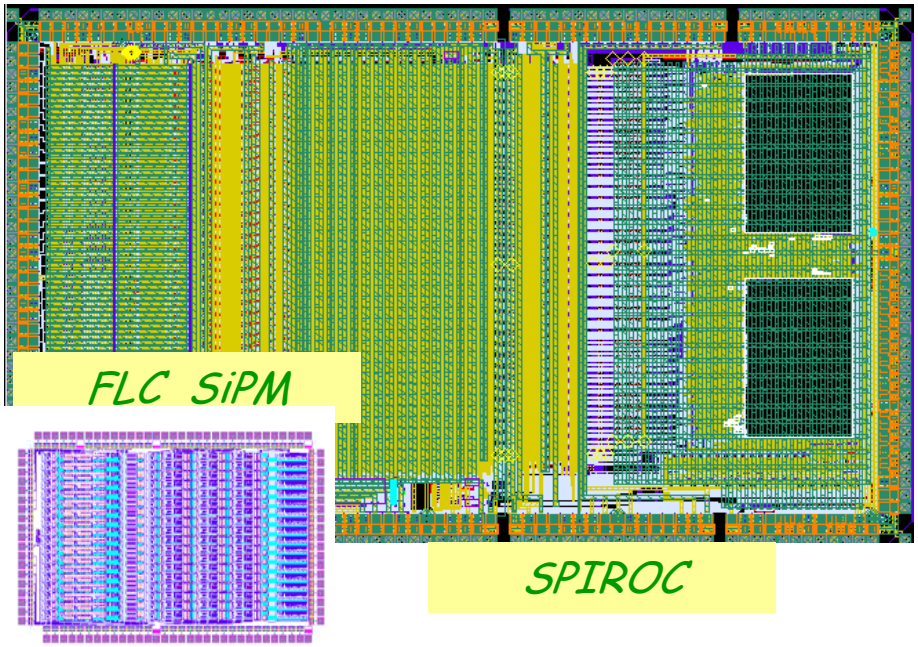
PMm² : large photodection area

- "PMm2" (2006 – 2009), funded by the ANR : **LAL, IPNO, LAPP and Photonis**
- **Replace large PMTs (20") by groups of smaller ones (12")**
  - central 16ch ASIC (MAROC like)
  - 12 bit charge + 12 bit time
  - water-tight, common High Voltage
  - Only one wire out (DATA + VCC)
  - Target low cost
  - Reuse many parts from MAROC & SPIROC
- **Application : large water Cerenkov neutrino**
  - 1ns time resolution
  - High granularity
  - scalability



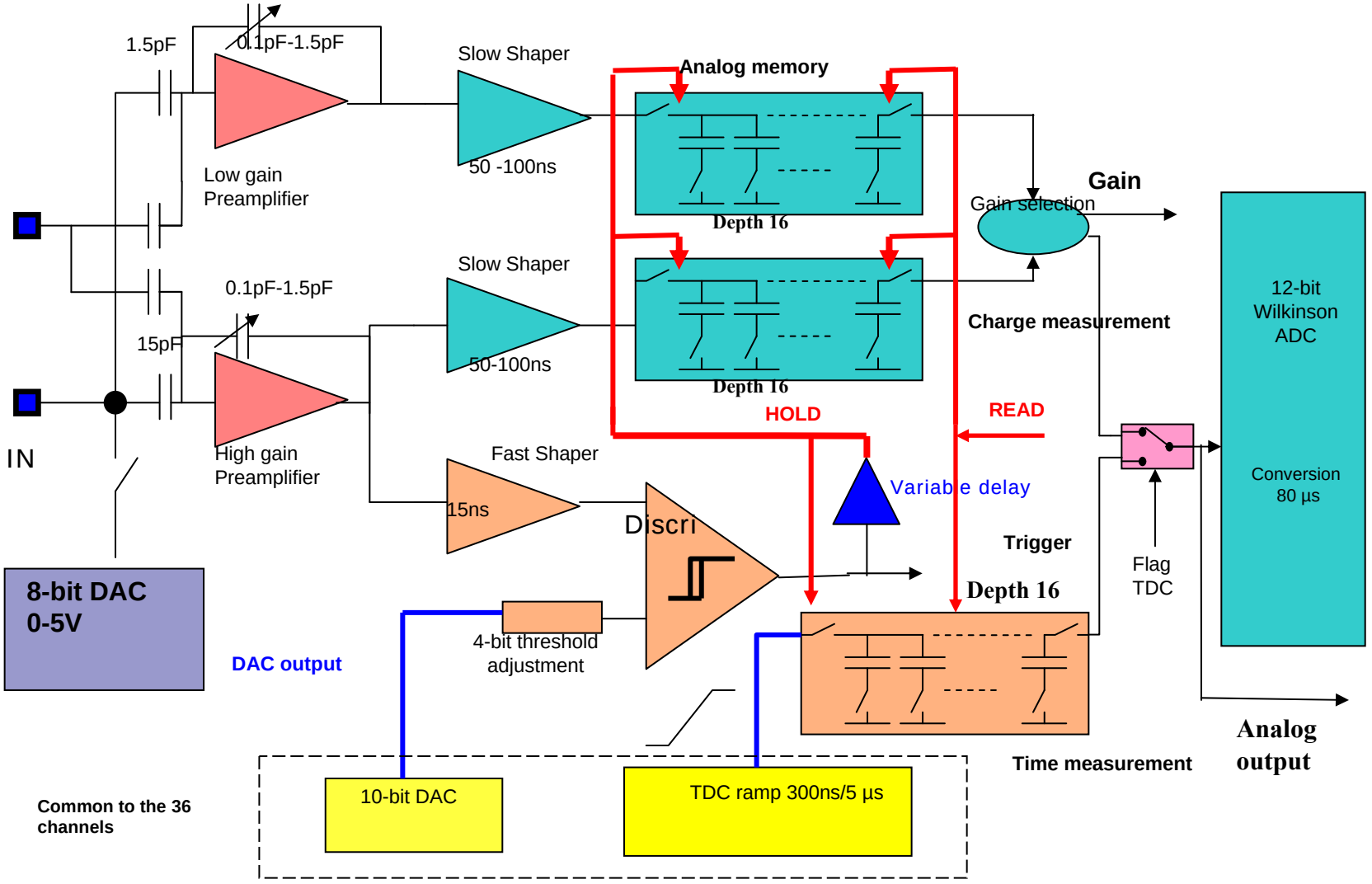
SPIROC : SiPM readout ASIC

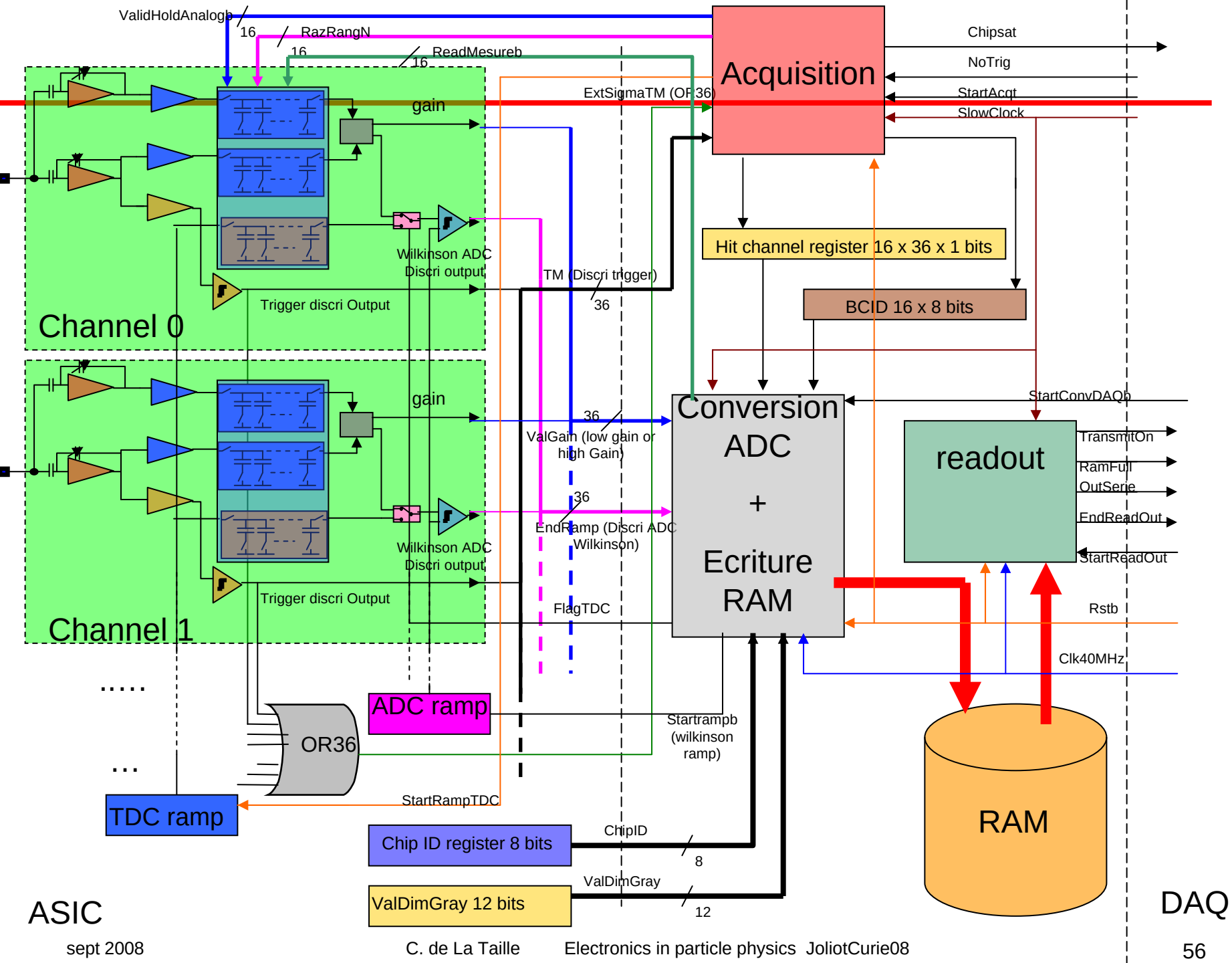
- **Silicon Photomultiplier Integrated Read Out Chip**
  - Evolution from FLCSiPM
  - 36 channels
  - Charge measurement (15bits)
  - Time measurement (< 1ns)
  - many SKIROC, HARDROC, and MAROC features re-used
  - Submitted in june 07 in SiGe 0.35 µm AMS



- **Collaboration with DESY for ILC hadronic calorimeters**
  - 9000 channels used in test beam in 2004-2008
  - Production in 2009 for Eudet module

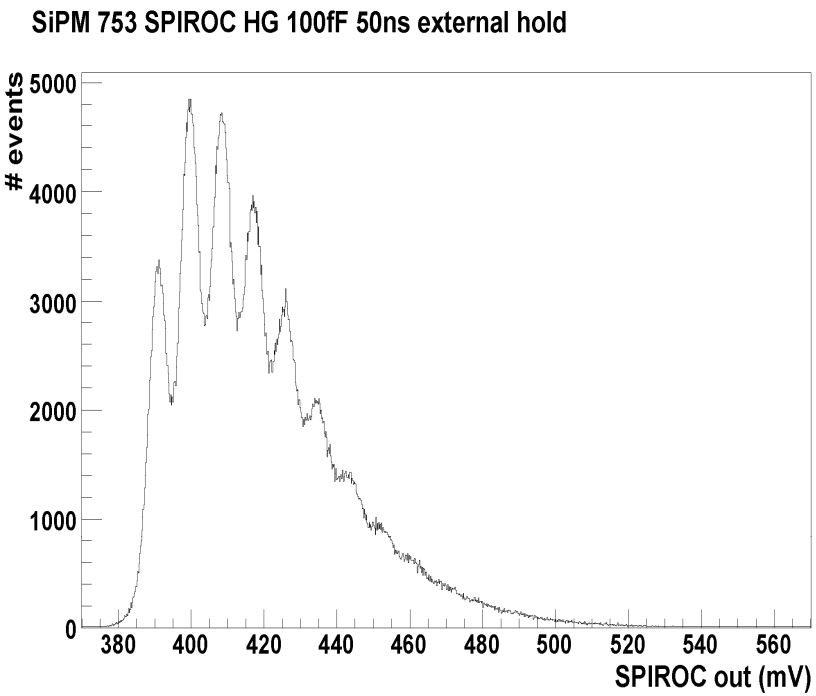
SPIROC : one channel

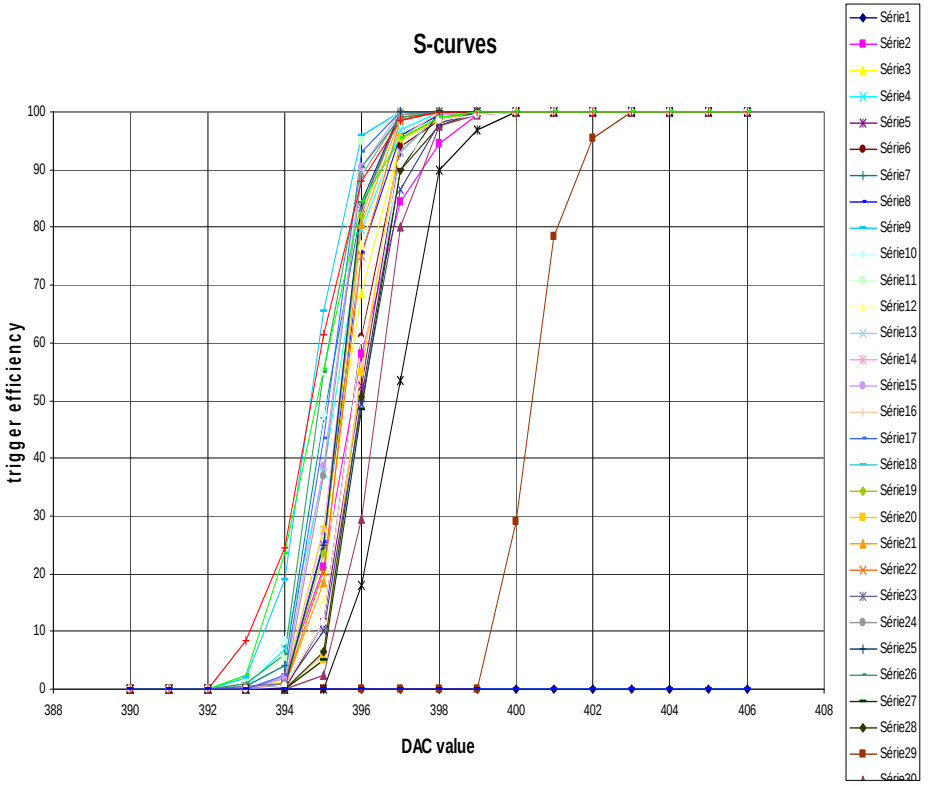



ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Channel 1
Wilkinson ADC
Discri output
Trigger discri Output
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray 12 bits
ValDimGray
12
RAM
ASIC
DAQ

SPIROC performance

- **Good analog performance**
  - Single photo-electron/noise = 8
  - Auto-trigger with good uniformity
  - Complex chip : many more measurements needed

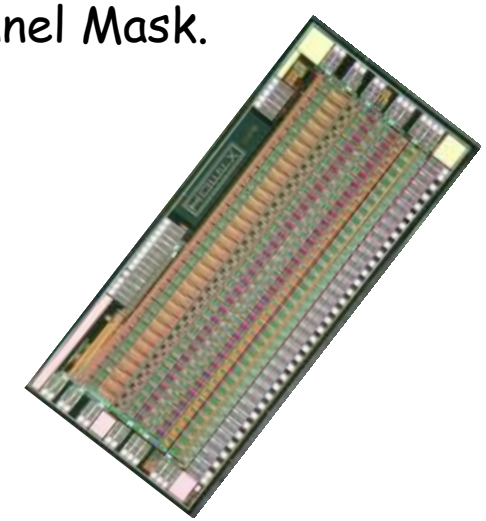


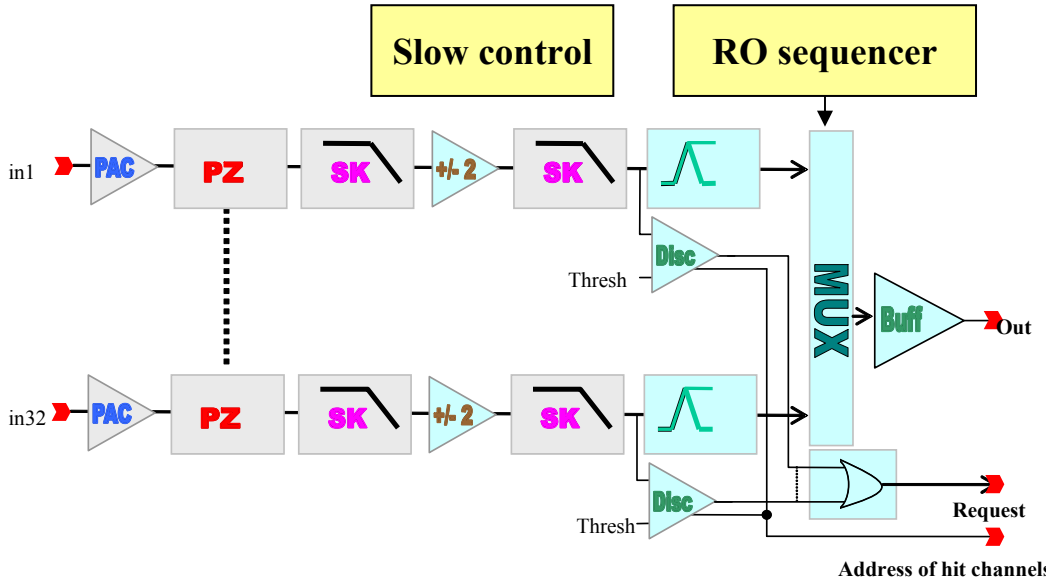


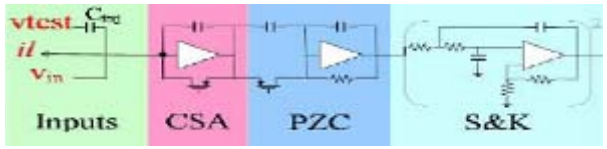
Idef-X 2.E for ECLAIRs.

-32 channels. Muxed output
-2.2 mW/ ch.
-Slow control => many parameters tunable
-Self triggered /1 Thresh/channel.
- 1µs-10µs selectable shaping.
-deal with both signal polarities.
-Peak detector, ~200mV/fC.
-sparsification and « smart » readout.

-Detector Leakage comp.
-Test/Calib inputs
-Channel Mask.







Idef-X: performances

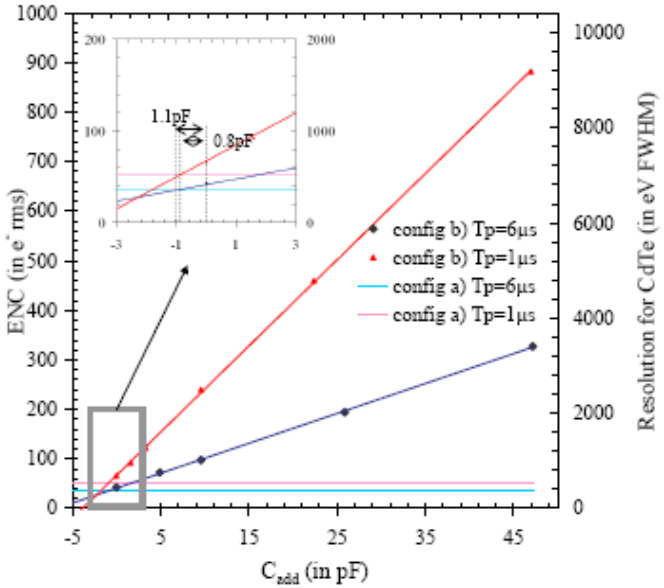
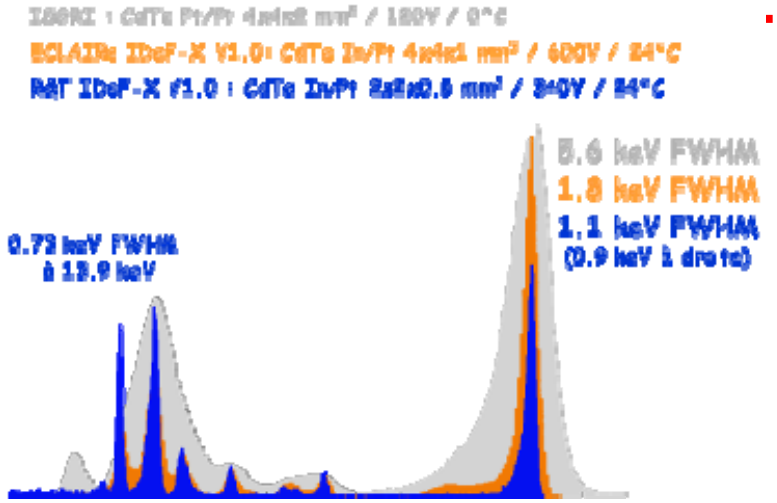


Fig. 4. Influence of the input additional capacitance. As expected, the lowest sensitivity of the chip to the input capacitance on its noise performance is obtained at the highest peaking time: at 6µs, the slope is evaluated to 6e⁻/pF. The comparison of these plots with the ENC values obtained in config (a) is done to extract the parasitic capacitance of the



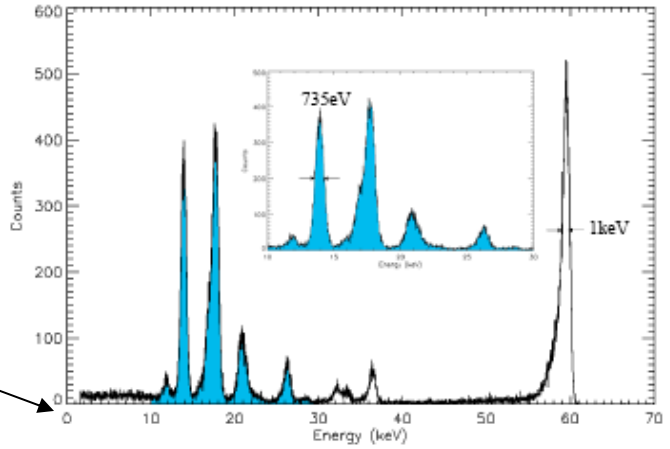


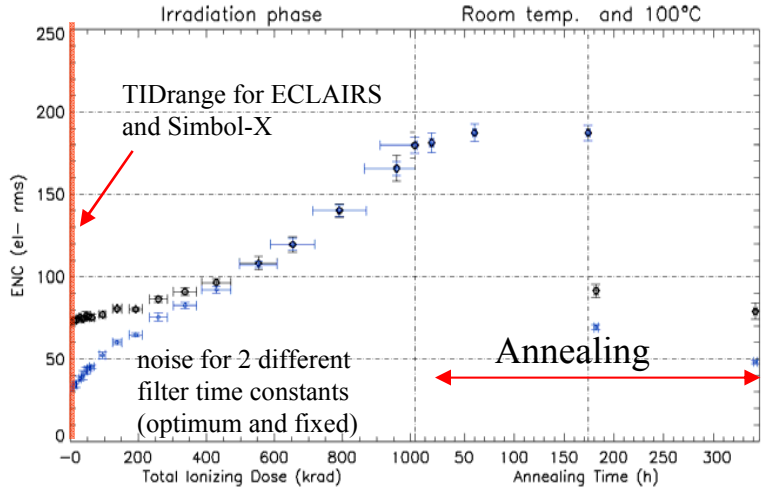
Fig. 6. Spectrum of an ^{241}Am source obtained with a 4.1 × 4.1 × 0.5 mm^3 CdTe detector equipped with a Schottky contact at the anode. The cathode is 2 × 2 mm^2 pixel surrounded by a 1 mm guard ring. The detector is biased under 330 V at 22°C and is connected to the channel #8 of IDeF-X V1.0 at a 6µs peaking time. The best spectrum is obtained at the highest peaking time because of the very low leakage current of the detector.

Low Thresh. << 4keV

Production for flight model out from fab in may 2008

IDeF-X family : radiation hardness.

- **IDeF-X V1.0**
  - TID: Irradiation with 60CO @ 500rad/h up to 1 Mrad

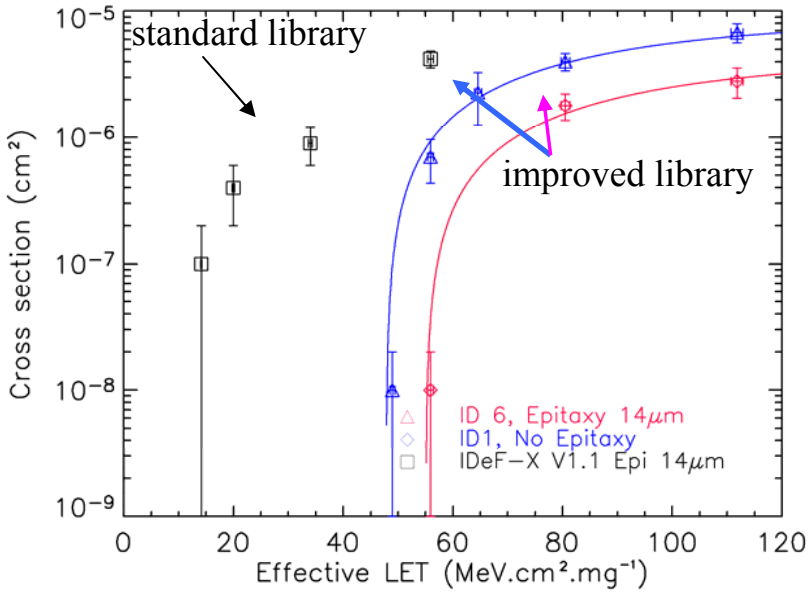


- **Up to 1 Mrad: no visible effect excepted on noise performances => Noise increase cleared by annelaing.**

For ECLAIRs and SIMBOL-X

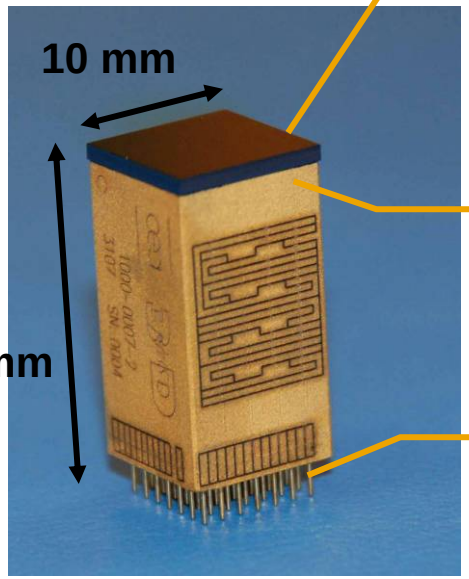
New digital library to improve hardness against SEL:

Test on Idef-X V2.E => no anti latchup circuit required for the ECLAIRs mission.



CALISTE 64 : 3D Xray microcamera for SIMBOL-X

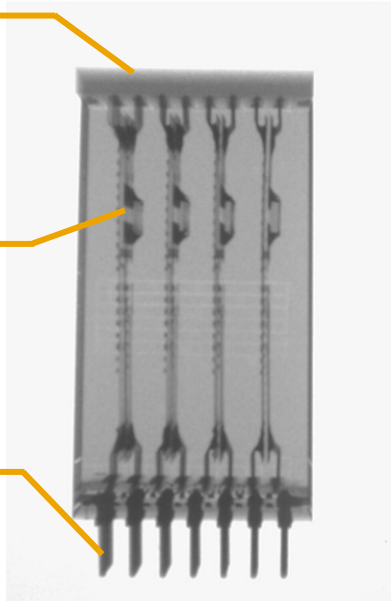
- A hybrid component based on a 3D Plus space proof technology.



CdTe detector
(64 pixels, 1mm pitch, 1mm thick, guard ring)

Front-end electronics
(4 IDeF-X 1.1 ASIC of 16 analogue channels)

Rear interface
(7x7 pin grid array, 1.27 mm pitch)

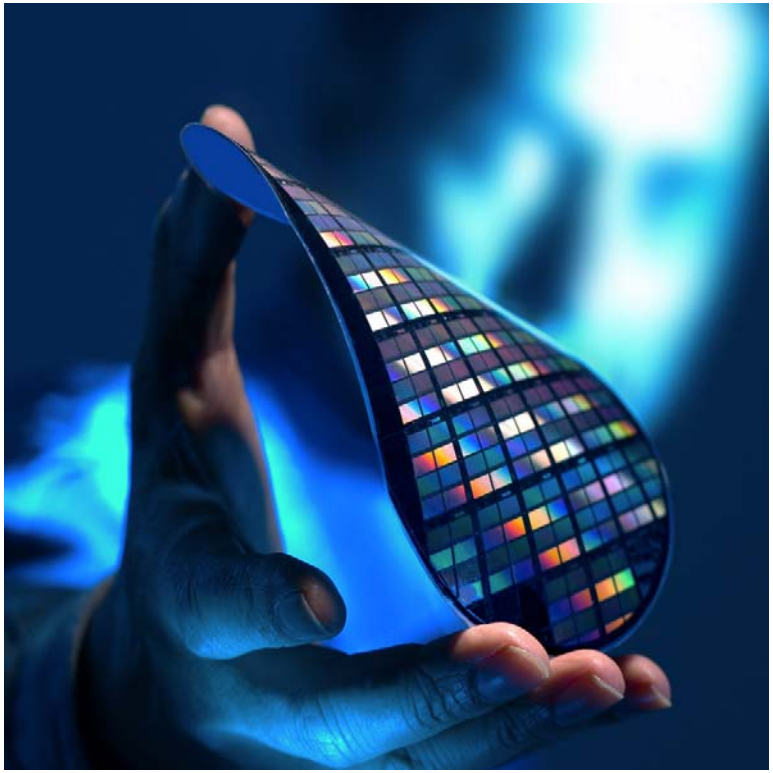


X radiography

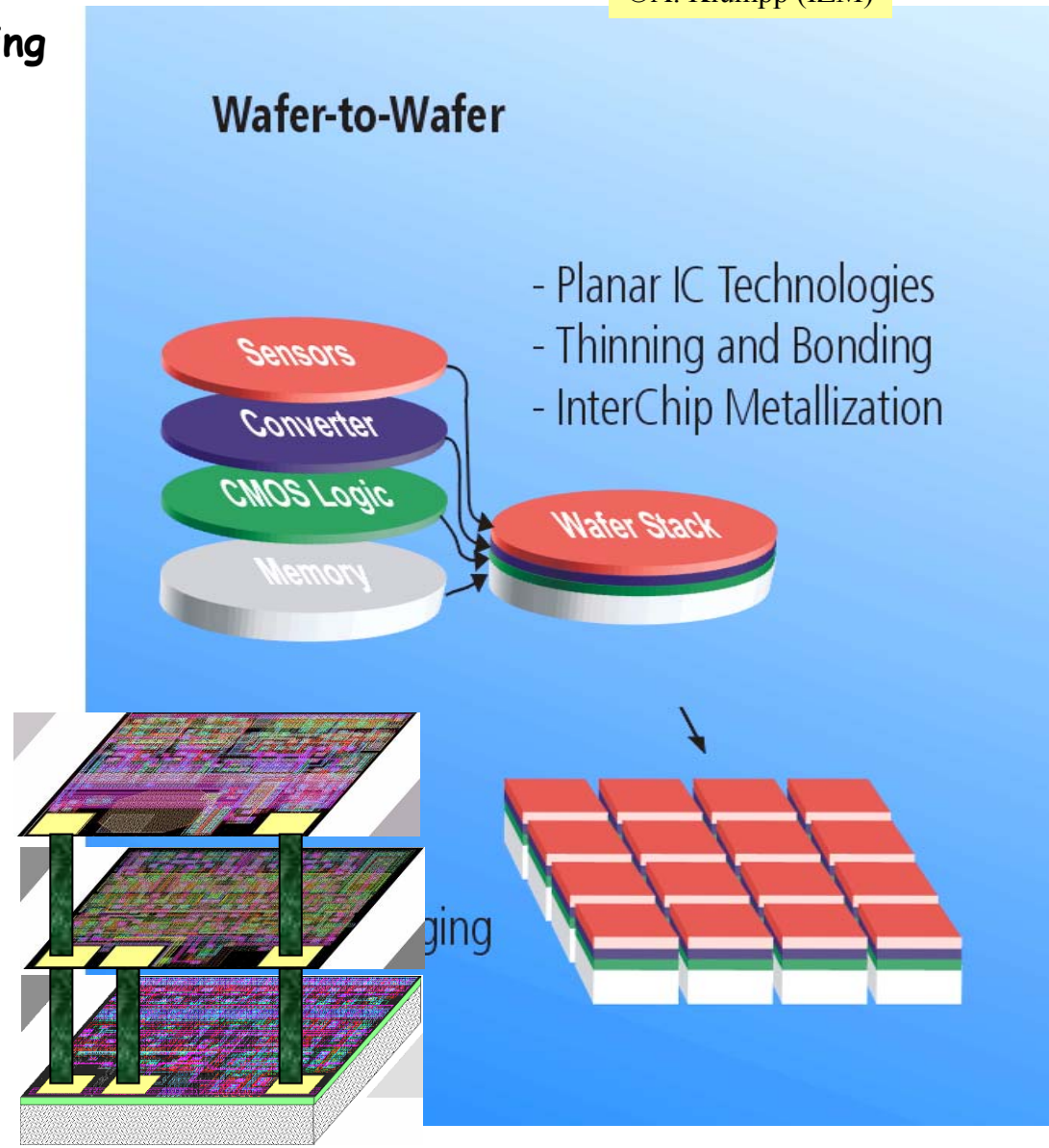
- Four micro PCB perpendicular to detection plan.
- Four ASICs to read out 2 rows of eight pixels each.
- Lateral routing to share signals between ASICs.

3D technology

- Increasing integration density, mixing technologies
- Wafer thinning to <50 µm
- Minimization of interconnects
- Large industrial demand
  - Processors, image sensors…

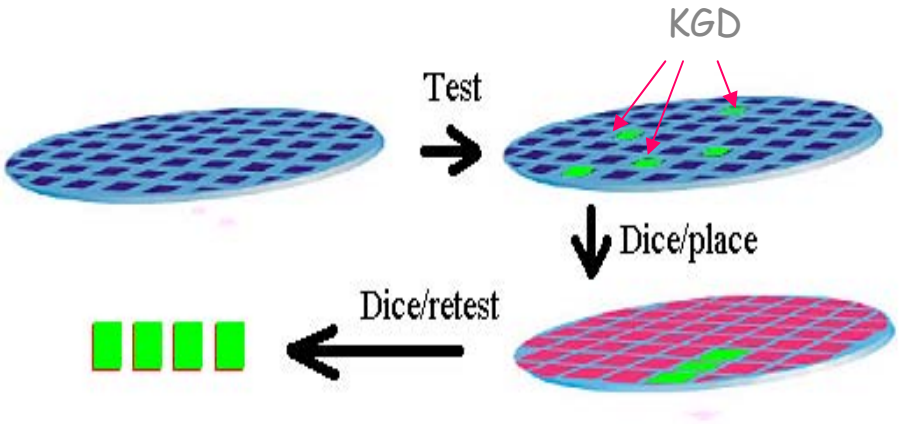


©A. Klumpp (IZM)

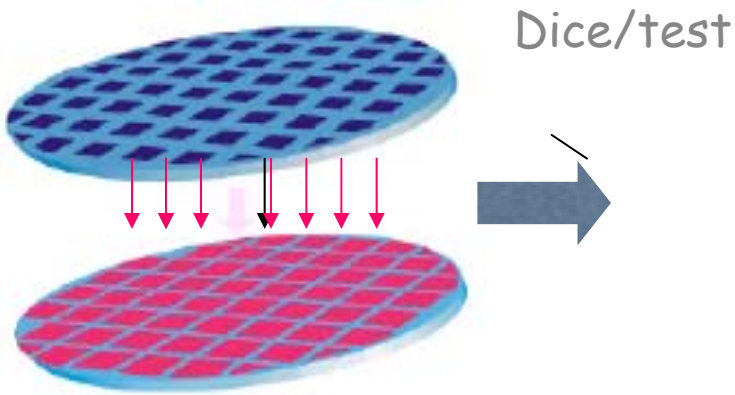


3D technologies

- **Wafer stacking**



Die to Wafer



Wafer to Wafer

Die to Wafer bonding
- Permits use of different size Wafers
- Lends itself to using KGD (Known Good Die) for higher yields

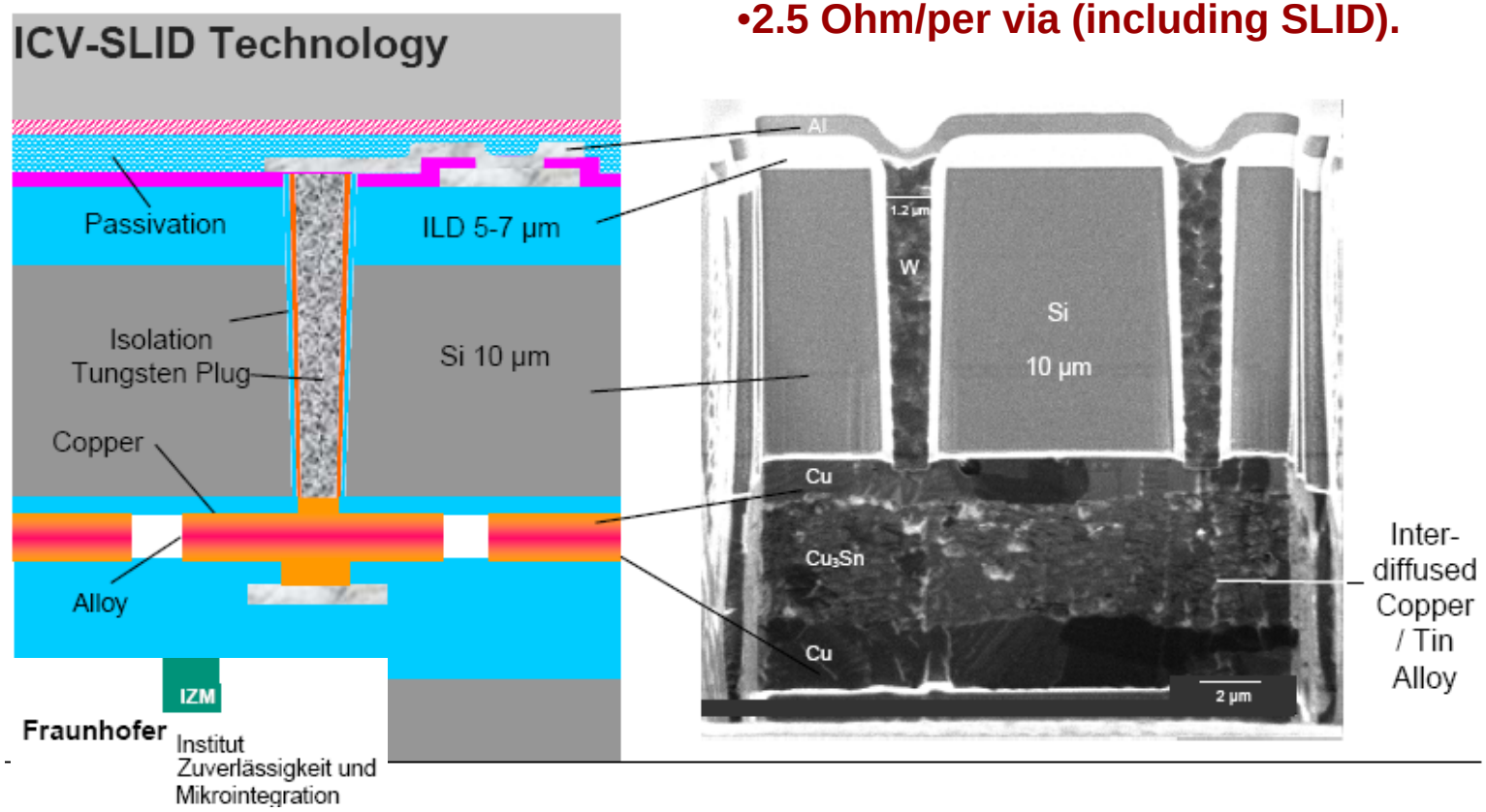
Wafer to Wafer bonding

- - must have same size wafers
- - Less material handling but lower overall yield

ICV : Inter-Chip vias

- Processes « via first » and « via last »
- Diameters : 1 µm to 50 µm
- Aspect ratio ~10

•Hole etching and chip thinning
•Via formation with W-plugs.
•Face to face or die up connections.
•2.5 Ohm/per via (including SLID).



Conclusion

- **A real move towards "smart sensors"**

- **micro-electronics getting closer to detector**
  - Unavoidable with increase of channels number
  - Cost reduction

- **Backend more and more integrated**
  - Integration of ADC
  - Signal processing
  - Loading of parameters

- **Coming up : 3D integration**
- **4-side abuttable sensors**